Electronic products industry supply chain: Summary of four phases of research efforts for conversion to lead-free electronics design and manufacturing

University of Massachusetts Lowell
Toxics Use Reduction Institute

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Electronic Products Industry Supply Chain: Summary of Four Phases of Research Efforts for Conversion to Lead-free Electronics Design and Manufacturing

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The Toxics Use Reduction Institute is a multi-disciplinary research, education, and policy center established by the Massachusetts Toxics Use Reduction Act of 1989. The Institute sponsors and conducts research, organizes education and training programs, and provides technical support to promote the reduction in the use of toxic chemicals or the generation of toxic chemical byproducts in industry and commerce. Further information can be obtained by writing the Toxics Use Reduction Institute, University of Massachusetts Lowell, 600 Suffolk Street, Suite 501 Wannalancit Mills, Lowell, MA 01854.

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Academic Research Program

The Academic Research program is a project of the Toxics Use Reduction Institute (TURI). The program connects the research capabilities of the University of Massachusetts with the emerging needs of Massachusetts manufacturers and the Commonwealth, to advance the investigation, development and evaluation of sustainable technologies that are environmentally, occupationally and economically sound. The program provides research funding to UMass faculty from all campuses, annually, on a competitive basis and encourages faculty/industry partnerships and cross-campus collaboration. Industry partners provide guidance, propose applications for new technologies and, in some cases, evaluate and/or adopt processes and technologies resulting from research. Past projects supported by this program have focused on finding alternatives to the use of toxic chemicals in various plastics applications. These projects are described in more detail on TURI's website (www.turi.org and click on Research, Academic Research Program).

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ABSTRACT

Although lead is a well-established human and environmental hazard, it is still used in electronic products on the printed circuit board surface finish, the finish of electronic components, and the solder that attaches the components to the board. Switching from lead-based materials to non-lead alternatives presents a significant challenge for the entire electronic products industry supply chain—from small assembly shops to large original equipment manufacturers. A major challenge with the new lead-free solder materials is higher melting temperatures, which require reflow ovens and other processing equipment to operate at higher temperatures.

The use of lead poses significant hazardous occupational exposure to workers in the electronic products industry, and also causes environmental challenges at the end of product life. For more than a decade, there has been a global effort in the electronic products industry to move towards using lead-free materials for the production of printed circuit boards. However, there were technical and economic challenges, such as long-term reliability and rework capability, that hindered the universal implementation of lead-free materials. As a result, many electronic products are still manufactured and assembled using materials containing lead.

The costs for investigating and evaluating the various lead-free electronic materials and manufacturing processes can be prohibitive for an individual company to undertake alone. Consequently, the Toxics Use Reduction Institute (TURI) and the University of Massachusetts Lowell formed the New England Lead-free Electronics Consortium as a collaborative effort of New England companies spanning the electronic products supply chain to help move the industry towards lead-free electronics. The Consortium is a working collaboration of industry, government, and academia. A major benefit is that contributions by the various consortium members made the research initiative cost effective. Many consortium members, especially smaller companies, could not have undertaken the effort as a sole entity due to funding constraints.

The Consortium has been successful in researching, identifying, developing, and testing lead-free materials and processes to address the challenges of assembly, rework, and long-term reliability challenge of lead-free electronics. The Consortium conducted four phases of research during the time period of 2001 through 2011. This paper presents a summary of the research approach and results achieved for all four phases of this research.

1.0 OVERVIEW

Although lead is a well-established human and environmental hazard, it is still used in many products such as batteries, cables, ammunition, fishing sinkers, wheel weights and electronic products. In electronic products, lead solder and surface finishes has remained the material selection of choice on printed circuit boards (PCBs) for the past sixty years because it is proven to work. The toxic substance has been commonly used on the boards in three areas: the board surface finish, the finish of electronic components, and the solder that attaches the components to the board. Manufacturers are moving away from using lead in electronic products for two main reasons: regulatory and market drivers.

Regulatory Drivers: A significant regulatory driver is the European Union's "Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS) Directive enacted in 2003. This directive restricts the use of lead in consumer electronic products.

Market Drivers: Although the RoHS Directive only affects companies who sell products in Europe, many major corporations have transformed their entire consumer product lines to avoid higher costs for maintaining two production lines—lead-free for European markets, and lead for other markets. Progressive companies that are exempt from RoHS because they provide mission-critical products (such as for the defense, medical, and aerospace industries) are also requiring suppliers to provide environmentally friendly products. This market demand cascades throughout the entire supply chain that now needs to provide materials, components, and assemblies that are lead-free or risk losing the business of the progressive companies.

Technical Challenges: Switching from the proven lead-based materials to non-lead alternatives presents a significant challenge for the entire electronic products supply chain industry—from small assembly shops to large original equipment manufacturers. A major challenge with the new lead-free solder materials is higher melting temperatures, which require reflow ovens and other processing equipment to operate at higher temperatures. This elevated temperature generates additional thermal stress and can damage components and circuit boards. With a narrower "processing window," which means much tighter manufacturing controls and standards, there is also a greater risk of mistakes that could be amplified throughout the supply chain. There are other technical challenges, such as long-term reliability and rework capability, that hinder the universal implementation of lead-free materials.

Environment, Health and Safety: The use of lead poses significant hazardous occupational exposure to workers in the electronic products industry and throughout the supply chain, and also causes environmental challenges at the end of product life. There are particular concerns during the recycling and disposal phase of the product life. Potential worker exposure from disassembly, grinding, burning and other recycling activities were a major reason for the European Union to pair their Waste Electrical and Electronic Equipment Directive with the RoHS Directive. Examples of illegal recycling and disposal activities causing egregious exposures and environmental contamination in developing countries have further driven the need to eliminate lead and other toxics from electronic products.

Cost of Changing: The costs for investigating and evaluating the various lead-free electronic materials and manufacturing processes can be prohibitive for an individual company to undertake alone.

Consequently, the Toxics Use Reduction Institute (TURI) and the University of Massachusetts Lowell formed the New England Lead-free Electronics Consortium as a collaborative effort of New England companies spanning the electronic products supply chain to help move the industry towards lead-free electronics. The Consortium is a working collaboration of industry, government, and academia. For the past several years, the Consortium has conducted research and testing for using various lead-free materials for the manufacture of printed circuit boards.

The Consortium has been successful in researching, identifying, developing, and testing lead-free materials and processes to address the challenges of assembly, rework, and long-term reliability of lead-free electronics. The Consortium conducted four phases of research from 2001 through 2011. This paper presents a summary of the research approach and results achieved for all four phases of this research.

The Consortium has previously completed and published the results for each of the four phases of manufacturing and testing of lead-free printed circuit boards with the goal of achieving lead-free soldering processes with quality and reliability equal to or better than that of leaded solder processes. Phase I was a screening-level research phase that examined various solder alloy combinations and reflow profiles. Phase II research was focused more broadly on processing parameters, utilizing a mix of component types and finishes in combination with five different printed circuit board finishes, two reflow atmospheres (air and nitrogen) and three solder paste compositions based on the same tin/silver/copper (Sn/Ag/Cu or SAC) alloy.

The primary goal of Phases I and II was to research different lead-free soldering alloys and processing parameters, and collectively agree on methods for assessing the visual quality, mechanical properties, and reliability of the resultant solder joints. Quality was examined by inspecting the lead-free solder joints, and reliability was established by thermal cycling the test vehicles and then pull testing the solder joints. All testing efforts were conducted according to IPC (Association Connecting Electronics Industries) standards. Comparisons to the baseline leaded joints were made, and the consortium members were satisfied that the lead-free soldering process is equivalent in quality and functionality to the leaded legacy solder process. Once the best performing solder alloys and processing method were established, research continued on to use these parameters on production test vehicles.

The goal of the Phase III effort was to focus on manufacturing and assembly issues by simulating an actual production board for parameters such as board layers, board size, and component density. The Phase III test vehicle was a twenty-layer board with components on both sides, populated with 1,750 components. The quality and reliability test methodologies established in earlier phases were applied to these production density boards. To better understand the reliability of the lead-free and tin/lead solder joints, thermal cycling and Highly Accelerated Life Testing (HALT) was conducted on the Phase III boards.

The goals of Phase IV were to expand the reliability testing by adding mechanical vibration testing, as well as specialized components that the consortium members wanted to test their solder joint quality and reliability. In addition, new materials that became available were also included in Phase IV, such as a nano surface finish, as well as new halogen-free board laminate materials. A new test vehicle was designed and used to evaluate different component types, surface finishes, laminates, and solder materials. The Phase IV research efforts were intended to address outstanding issues such as rework and long-term reliability when using lead-free solder materials.

The following table provides a summary of the four research phases.

Table 1.1.: ***Lead-free Electronics Research Summary***

Phase	Test Vehicle (Experimental Printed Circuit Board)	Factors Investigated	Results
Phase I 2001-02	Experimental Board: Single layer, single sided, surface mount components only, low component density.	LF solder alloys (3) Thermal profiles (3) Reflow environments (3) Surface finishes (2)	• Lead-free soldering with equal or fewer defects than lead soldering is possible with experimental boards. • After thermal cycling, the quality and strength of lead-free solder joints is comparable to lead solder joints for experimental boards. • Decision to focus on SAC alloy and a ramp to peak thermal profile for reflow processes.
Phase II 2002-04	Experimental Board: Single layer, single sided, surface mount components only, low component density.	LF Solder pastes (3) Thermal profiles (1) Reflow environment (2) Surface finishes (5)	• Decision to focus on air only atmosphere for reflow environment. • Decision to focus on 3 printed circuit board surface finishes: ENIG, OSP, and Immersion silver.
Phase III 2004-07	Production Density Board: 20 layers, double sided, surface mount and through-hole components, high component density.	LF Solder pastes (2) Thermal profiles (1) Reflow environment (1) Surface finishes (3) Laminate materials (2)	• Addition of HALT for quality and reliability testing. • Lead-free soldering with equal or fewer defects than lead soldering is possible for production like boards. • Decision to use Isola HR370 laminate material as baseline lead-free laminate material for upcoming experiments.
Phase IV 2008-11	Production Density Board: 20 layers, double sided, surface mount and through-hole components, high component density.	LF Solder pastes (3) THT solder materials (2) Thermal profiles (1) Reflow environment (1) Surface finishes, including one with nanomaterials (4) Laminate materials including halogen and non-halogen (2)	• Addition of newly available materials (e.g. nano surface finish and halogen free laminates) and vibration testing. • Successful single and double rework efforts are possible with lead-free materials that can achieve Class 3 standards without signs of thermal degradation. • Long-term reliability results of lead-free materials were mixed for the various component types investigated. • The halogen-free laminate materials had early failures during thermal cycling and require reformulation before additional reliability testing.

Consortium members contributed their resources to find lead-free alternatives. TURI estimates the cost for materials, supplies, testing equipment usage, production equipment usage, engineering support, inspection services, and technical expertise provided by the companies and organizations to total more than $1.5 million for the four phases of research.

The Consortium has been a success because of the willingness of the companies to share their technical knowledge, contribute resources, materials and equipment, and collaborate with government and academia towards a common goal of transitioning the industry to lead-free electronics. The following companies and organizations contributed resources for one or more of the four phases of the Consortium research:

- AIM, Montreal, Canada
- Air Products and Chemicals, Allentown, PA
- American Power Conversion, Billerica, MA
- Analog Devices, Wilmington, MA
- Benchmark Electronics, Nashua, NH
- BTU International, Billerica, MA
- Cobham DES-M/A-COM, Lowell, MA
- DDI, Sterling, VA
- EMC, Hopkinton, MA
- FreedomCAD, Nashua, NH
- Hadco Corporation, Haverhill, MA
- International Rectifier, Leominster, MA
- Isola, Chandler, AZ
- Multicore Solders, Richardson, TX
- Ormecon, Ammersbek, Germany
- PWB Interconnect Solutions, Ontario, Canada
- Raytheon, Tewksbury, MA
- Schneider Electric, N. Andover, MA
- Skyworks, Woburn, MA
- Solectron, Westborough, MA
- Stentech, Salem, NH
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- Textron Systems, Wilmington, MA
- Toxics Use Reduction Institute, Lowell, MA
- U.S. EPA, Boston, MA
- University of Massachusetts, Lowell, MA
- Vitronics Soltec, Stratham, NH
- Wall Industries, Exeter, NH
- Yankee Soldering, E. Greenwich, RI

2.0 INTRODUCTION

2.1 Use of Lead in Electronics

Since the emergence of etched printed circuit board technology, lead has been used in a variety of ways for manufacturing printed circuit boards. Lead can be used as a conductive surface finish on printed circuit boards, as a conductive component finish, as solder paste for the assembly of surface mount components, and as bar solder for assembly of through-hole components. Lead is used as a material in electronic products because it has many desirable properties such as a low melting temperature and low cost, and also because it forms reliable solder joints. [1]

Printed circuit boards are found in electronic products. The printed circuit board is crucial to the manufacture and sales of approximately $1 trillion in electronic products each year. The printed circuit board is the platform upon which electrical components such as semiconductor chips and capacitors are mounted, and it provides the electrical interconnections between components. In 2003, the United States produced approximately 15% of the world's printed circuit boards. [2] In the United States during 2003, approximately 13.9 million pounds of lead were used in solder for the manufacture of electronic products [3]

2.2 Hazards of Lead

The acute and chronic toxic effects of lead to humans have been well studied. The U.S. EPA considers lead to be a Group B2, "probable human carcinogen." [4] The International Agency for Research on Cancer (IARC) considers lead to be Group 2B, "possibly carcinogenic to humans." [5] Because of the multi-modes of action of lead in biological systems, lead can potentially affect any system or organ in the body, although the most sensitive targets are the urinary, hematological, cardiovascular, and nervous systems. Acute exposure to high levels of lead causes brain damage, kidney damage, and gastrointestinal distress. Studies on male lead workers have reported severe depression of sperm count and decreased function of the prostate and/or seminal vesicles. Occupational exposure to high levels of lead has been associated with a high likelihood of spontaneous abortion in pregnant women. Exposure to lead during pregnancy produces toxic effects on the human fetus, including increased risk of preterm delivery, low birth weight, and impaired mental development. Neurological symptoms have been reported in adults with elevated blood lead levels of greater than 40 µg/dL. [6]

Approximately 99% of the amount of lead entering a human adult body will be expelled in urine or fecal waste within a few weeks, but only about 32% of lead entering a child's body will be excreted. Continued exposure will result in accumulation of lead in body tissues. [4]

The use of lead materials in electronic products potentially exposes workers in companies throughout the entire supply chain: transportation, solder and solder paste manufacturing, electronic component manufacturing, circuit board manufacturing, assembly of circuit boards, final product assembly, use and repair of electronic products, recycling of electronic products, and disposal of electronic products.

Illegal recycling and disposal activities have caused significant exposures and environmental contamination in developing countries.

Human exposure to lead typically occurs through a combination of inhalation and oral exposure. For companies that are involved with circuit board assembly operations, inhalation of lead can occur during soldering processes. The primary solder operations occur during reflow soldering of surface mount components, wave soldering of through-hole components, and manual soldering of reworked components.

The Leadout Project is a European funded initiative to help companies across Europe develop technological solutions for implementing lead-free solutions in the electronic products industry. [7] A study was conducted by the Leadout Project to measure the occupational exposure to lead during reflow and wave soldering operations. Occupational exposure measurements were performed at three different electronic products companies using personal sampling pumps in the breathing zone of workers who were conducting reflow and wave solder operations using tin/lead solder. The action level limit (30 $\mu g/m^3$) was exceeded by two out of the three companies for reflow solder operations, and the permissible exposure limit (50 $\mu g/m^3$) was exceeded by two out of the three companies for wave solder operations. The lead emission results from this study are shown in the table below. [8]

Table 2.1: ***Lead Emission Measurements (Aguirre, 2006)***

Company	Wave Solder: Lead Exposure ($\mu g/m^3$)	Reflow Solder Lead Exposure ($\mu g/m^3$)
IDK (Spain)	68	30
ALCAD (Spain)	18	16
TELCA (Portugal)	115	< 33

During the many and varied processes of electronic assembly, there is considerable handling of lead solder, lead solder paste, components with lead finish, and circuit boards with lead finish. For example, the printing operator must pick up circuit boards with a lead finish, as well as manually apply lead solder paste to the printing machine. The handling of these lead-containing materials can result in lead contamination of workers' hands and clothing. This contamination of hands and clothing can ultimately cause lead ingestion if proper hand and clothing washing procedures are not conducted. Ingestion of lead can also occur through contact with lead-contaminated hands, food, cigarettes, and clothing. Further, lead-contaminated clothing and other objects that are brought into the home environment also represent a potential exposure hazard to occupants in the home, especially to children. [9]

The environmental hazards involved with the use of lead solder in electronic products often occur during the disposal stage. At the end of life, electronic products often end up at incinerators, landfills, or dumping areas. Incinerators without proper control technology can allow lead to enter the ambient atmosphere; landfills or dumping areas that are not properly lined can allow the migration of lead to soil and groundwater. In situations where waste is well managed, millions of pounds of lead are still deposited in solid waste and incinerator ash landfills. In Massachusetts alone, waste incinerators annually generate approximately 2 million pounds of lead that must be disposed of.

2.3 Drivers of Lead-free Electronics

For the past decade, there has been a global effort in the electronic products industry to initiate a move towards using lead-free materials for the production of printed circuit boards, driven by regulations and the market. A major regulatory driver has been the European Union's Restriction of the Use of Certain Hazardous Substances (RoHS) Directive that was enacted in 2003. This directive limits the amount of lead and five other substances that are used in consumer electrical and electronic equipment. This directive covers some, but not all, electrical and electronic equipment placed on the European Union (EU) market as of July 2006. There are several types of electronic products (e.g. medical equipment, aerospace, etc.) that are either exempt or considered out of scope from the original directive, however, the EU is expected to gradually phase many of them in under future RoHS Directive updates.

Even in the absence of regulatory requirements, several companies have responded to market drivers to eliminate lead from their electronic products. Many progressive companies are trying to produce more environmentally friendly and recyclable products, as well as providing a safer working environment for their employees. In addition, lead-free is becoming the standard for most consumer products because of international regulations, and maintaining both lead and lead-free process and product lines is costly and increases the likelihood of errors or cross-contamination.

2.4 Challenges of Lead-free Electronics

Despite the environmental and occupational hazards described in the preceding section, there is continued use of lead solder. There are many reasons for this practice, including technical and economic challenges in transitioning to lead-free materials. A common source for many of these challenges is that the melting temperature of lead-free solders is typically higher than that of tin/lead solder. Specifically, the melting temperature of tin/lead solder is 183 ^{o}C, and the melting temperature of SAC solder (a common lead-free solder material) is approximately 217 ^{o}C. Therefore, the manufacturing process equipment must be run at higher temperatures. For surface mount components, the reflow oven temperature must be higher when using lead-free solder pastes. For through-hole components, the solder pot temperature must be higher for wave solder, selective solder, and rework machines when using lead-free solders.

The elevated temperatures necessary to accommodate lead-free solders pose technical challenges. Most common components and printed circuit board laminate materials are rated for the lower processing temperatures required for a tin/lead electronic products assembly environment. Increased processing temperatures can cause issues related to thermal stress such as printed circuit board delamination and component failure.

During the assembly of printed circuit boards, there is often the need to rework the boards due to failures or defects encountered during the assembly process. This rework involves the removal and replacement of components on the printed circuit board. Also, rework of printed circuit boards can occur anytime during the life of the electronic product. For example, if there are component failures during the use of the product, the printed circuit board may have to be sent back to the manufacturer for rework.

The elevated solder temperatures and solder flow required for rework of through-hole components can result in copper dissolution (the erosion of the copper thickness of the pad and barrel wall for plated through holes) on the printed circuit board. Copper dissolution can result in adverse effects on solder alloy performance, increase the required frequency for solder analysis, increase the required solder pot maintenance, and potentially compromise the long-term reliability of the printed circuit board.

The higher processing temperature of lead-free alloys generates more thermal stress to the printed circuit board. Also, the lead-free solders typically do not flow as well as tin/lead solders and need more contact time between the solder and the printed circuit board. This also generates additional thermal stress to the printed circuit board. Another issue with lead-free solders is that they have a higher tin content than tin/lead solders. The tin component of most solders reacts with the copper substrate and forms metallic connections known as "tin whiskers," which can cause potential electrical shorts.

The most challenging technical barrier to the widespread adoption of lead-free electronic products is the impact on the long-term reliability of the lead-free products. Lead solder has been used extensively for the past sixty years and there is a large reservoir of reliability data available. It has been proven that electronic products containing lead solder can have operational lives of twenty or more years. However, this reliability data has not yet been generated for lead-free electronics, and consequently there is reluctance to use lead-free materials for products that require a long operational life. Because of this, there are numerous electronic product applications that continue to use materials containing lead, such as network infrastructure, aerospace, defense, information technology, and medical devices. [10]

There are also economic barriers to the widespread adoption of lead-free electronics. For example, the most common lead-free solder used is a SAC alloy that is more expensive than tin/lead solder, mostly due to the silver content. Also, new circuit board laminate materials are needed to accommodate the higher processing temperatures, which are typically more costly than traditional materials. Another cost issue is the increased energy requirement that is necessary to operate the processing equipment at a higher temperature to accommodate the lead-free solder. A reflow oven processing lead-free assemblies uses approximately 20% more energy than for tin/lead PCB assemblies.

2.5 New England Lead-free Electronics Consortium

The costs of investigating and evaluating the various lead-free materials and manufacturing processes are usually prohibitive for an individual company to undertake alone. The New England Lead-free Electronics Consortium was formed as a collaborative effort of New England companies spanning the electronic products supply chain to help move the industry towards lead-free electronics. The Consortium has been initiated, sponsored, and supported by the Toxics Use Reduction Institute and the University of Massachusetts Lowell.

The Consortium is a working collaboration of industry, government, and academia. Companies in the electronic industry supply chain include original equipment manufacturers (OEMs), printed circuit board assemblers, electronic component suppliers, circuit board manufacturers, electronic products designers, and material suppliers. Results of a 2006 study conducted to examine the role of partnerships between OEMs and suppliers in improving the environmental performance of manufacturing operations support.

the benefits of this kind of collaborative approach. The results of the study indicate that the closer the relations, the greater the improved environmental performance of the companies involved. It was found that as suppliers learned more about the manufacturing operations of the end product, they were better able to understand the type of product that would best meet the needs of the end customer and innovate accordingly. [11] Significant opportunities exist along the supply chain to reduce a company's environmental impact, including substituting chemicals in order to reduce the generation and management of hazardous materials. [12]

For more than a decade, the New England Lead-free Electronics Consortium has conducted research and testing for using various lead-free materials for the assembly of printed circuit boards. The Consortium has been successful in researching, identifying, developing, and testing lead-free materials and processes to address the challenges of assembly, rework, and long-term reliability challenge of lead-free electronics. The Consortium conducted four phases of research during the time period of 2001 through 2011.

3.0 PHASE I RESEARCH EFFORTS

3.1 Overview

The Phase I screening level research was conducted in 2001 and 2002. Phase I provided an initial examination of various solder alloy combinations and reflow profiles for the manufacture of lead-free electronic assemblies. The key contributors for the Phase I research efforts included Dr. Sammy Shina and Hemant Belbase from the Department of Mechanical Engineering at the University of Massachusetts Lowell, Karen Walters from BTU International, Tom Bresnan from Sanmina Corporation, Peter Biocca and Tim Skidmore from Multicore Solders, David Pinsky from Raytheon Corporation, Phil Provencal from Solectron Corporation, Don Abbott and Ray Lizotte from Texas Instruments, and Liz Harriman from the Toxics Use Reduction Institute. This summary draws heavily from previous Phase I reports, including "Process and Material Selection for zero defects and superior adhesion Lead Free SMT soldering" by Shina, et al, published by Surface Mount Technology Association, [13] and “Reliability Testing Techniques for Lead-free Soldering of SMT Technology”, presented at the 2001 ETRONIX Conference. [14]

3.2 Experimental Design

A Design of Experiments matrix was developed by the Consortium members based on their collective electronic products manufacturing experience and the available resources and materials. The factors and levels selected for the experimental design were as follows:

1. Solder pastes: The following materials were selected based upon published performance data and actual use in consumer products.

- 96.5/3.5 Tin/Silver alloy (SnAg)
- 95.5/3.8/0.7 Tin/Silver/Copper alloy (SAC)
- 57/43 Tin/Bismuth alloy (Sn/Bi)
- 63/37 Tin/Lead alloy (Sn/Pb) for baseline comparisons

2. Printed circuit board surface finishes: The following materials were selected based on low price and wide use within the electronic products industry.

- Organic Solder Preservative (OSP)
- Electroless Nickel/Immersion Gold (ENIG)

3. Reflow atmospheres: Two reflow oven environments were selected to understand the possible effect on the reflow process.

- Air environment in the reflow oven
- Nitrogen (20 PPM Oxygen) environment in the reflow oven

4. Reflow process: In order to fully understand the impact of the reflow process, two factors were investigated: 1) Time Above Liquidus (TAL) and 2) reflow profile. Levels were selected to examine

the impact of lessening the thermal shock to the electronic components by trading off the lengthening of the reflow time (TAL) versus a lower peak temperature or applying a longer preheat exposure time to the reflow process (a linear or a cash register reflow profile).

- TAL: 60, 90 or 120 seconds
- Reflow Profile: linear (soak) or cash register profile

3.2.1 Test Vehicle

The test vehicle developed for the Phase I research was a 4 inch wide x 5.5 inch long FR4 glass reinforced epoxy laminate board (see Figure 3.1). A total of 66 test vehicles were assembled and tested. Fifty-four test vehicles were assembled with 100% lead-free solder materials, and twelve test vehicles were assembled utilizing a controlled tin/lead soldering process. A no clean, high residue, high activity flux was used with all four solder alloys.

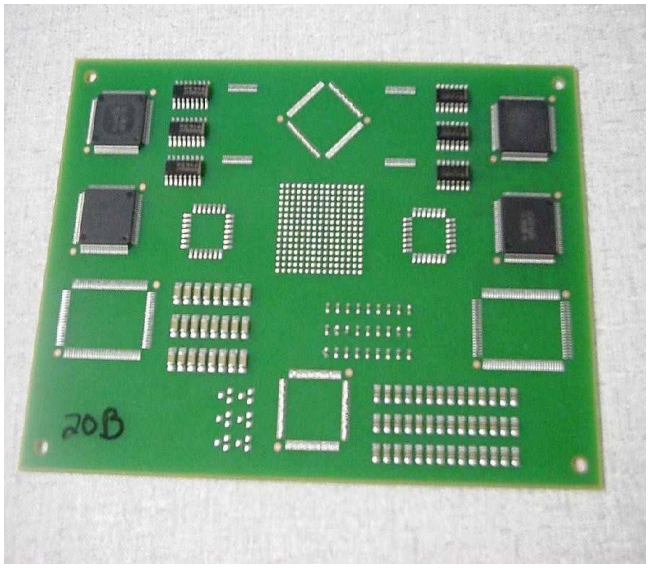

Figure 3.1. **Phase I test vehicle.**

3.2.2 Components

The baseline tin/lead solder test vehicles were built with components that had a tin/lead component finish and the experimental test vehicles were assembled with parts that had lead-free finishes. The lead-free resistor components were tin-plated and the lead-free integrated circuit components were plated with nickel palladium. Components assembled on each test vehicle included:

Resistor Components:

- 0805 resistors (quantity of 24)
- 0402 resistors (quantity of 18)
- 1206 resistors (quantity of 21)

Integrated Circuit Components:

- low profile quad flat package LQFP100s with 0.01977 pitch (quantity of 1)
- low profile quad flat package LQFP120s with 0.0157 pitch (quantity of 1)
- small outline package SO14s (quantity of 3)

3.2.3 Experiment Layout

Twenty-seven lead-free experiments were run examining the three alloys, two printed circuit board surface finishes, three different times above the melting point, two reflow oven profiles, and two reflow environments. For each experiment a sample size of two test vehicles was chosen. On each test vehicles, there were 1,279 visual defect opportunities (one for each solder joint on the test vehicle). Table 3.1 provides the parameters used for the Phase I lead-free solder test plan.

Table 3.1: ***Lead-free Solder Test Plan***

Run Number	Solder Paste	Surface Finish	Time Above Liquidus	Soak Profile	Nitrogen Atmosphere
1	Sn/Ag/Cu	OSP	60 sec	Yes	Yes
2	Sn/Ag/Cu	OSP	90 sec	No	No
3	Sn/Ag/Cu	OSP	120 sec	No	Yes
4	Sn/Ag/Cu	ENIG	60 sec	No	No
5	Sn/Ag/Cu	ENIG	90 sec	No	Yes
6	Sn/Ag/Cu	ENIG	120 sec	Yes	Yes
7	Sn/Ag/Cu	OSP	60 sec	No	Yes
8	Sn/Ag/Cu	OSP	90 sec	Yes	Yes
9	Sn/Ag/Cu	OSP	120 sec	No	No
10	Sn/Bi	OSP	60 sec	No	Yes
11	Sn/Bi	OSP	90 sec	No	Yes
12	Sn/Bi	OSP	120 sec	Yes	No
13	Sn/Bi	ENIG	60 sec	No	Yes
14	Sn/Bi	ENIG	90 sec	Yes	No
15	Sn/Bi	ENIG	120 sec	No	Yes
16	Sn/Bi	OSP	60 sec	Yes	No
17	Sn/Bi	OSP	90 sec	No	Yes
18	Sn/Bi	OSP	120 sec	No	Yes
19	Sn/Ag	OSP	60 sec	No	No
20	Sn/Ag	OSP	90 sec	Yes	Yes
21	Sn/Ag	OSP	120 sec	No	Yes
22	Sn/Ag	ENIG	60 sec	Yes	Yes
23	Sn/Ag	ENIG	90 sec	No	Yes
24	Sn/Ag	ENIG	120 sec	No	No
25	Sn/Ag	OSP	60 sec	No	Yes
26	Sn/Ag	OSP	90 sec	No	No
27	Sn/Ag	OSP	120 sec	Yes	Yes

To provide a baseline for comparison purposes, 12 test vehicles were assembled using tin/lead solder, tin/lead finish components, and a typical conventional tin/lead reflow profile. Table 3.2 provides the parameters used for the Phase I tin/lead solder test plan.

Table 3.2: ***Tin/Lead Solder Test Plan***

Run Number	Surface Finish	Reflow Environment
1	OSP	Nitrogen
2	OSP	Nitrogen
3	OSP	Nitrogen
4	OSP	Air
5	OSP	Air
6	OSP	Air
7	ENIG	Nitrogen
8	ENIG	Nitrogen
9	ENIG	Nitrogen
10	ENIG	Air
11	ENIG	Air
12	ENIG	Air

3.3 Visual Analysis Results

Visual inspection of the assembled test vehicles was performed according to the IPC J-STD-001industry standard. The inspectors used the visual inspection lens magnification settings up to 10x.

The lead-free solders did not seem to wet very well compared with the tin-lead solder. Most of the defects encountered were due to poor wetting and fillets. Since the flux used in the experiments was a no clean, high activity, high residue type, most of the boards had high flux residue. At first glance it could be observed that the solders did not reflow as expected, potentially due to the metallurgical behavior of the solders and surface finishes. Since wetting characteristics of the solder depend upon the metallurgy of the component lead and pad surface finish, this was anticipated. The OSP finished test vehicles seemed to have more defects than the ENIG finished boards. It was also observed that nitrogen did improve the wetting characteristic of the solder.

The tin-lead baseline generally behaved the same as the lead-free setup. Although the tin-lead solders showed fewer defects than the lead-free solders, they followed the same behavior for OSP and ENIG surface finishes and the nitrogen reflow environment. Statistical analysis of the results indicated that the significant factors were lead-free solder paste, printed circuit board surface finish and the reflow environment. All other factors were not significant in the visual defect performance of the test vehicles.

3.3.1 Mechanical Sources of Materials Failures

The mechanical reliability of lead-free solder joints is based on several properties of the solder materials: fatigue, creep, impact, and reforming of inter-metallic boundaries.

1. Fatigue: This can result in a sudden and catastrophic failure of the solder joint and is due to fluctuating load, deformation or embrittlement over time. Fatigue begins with a crack, and proceeds to grow until it becomes unstable. A major source of fatigue is thermal cycling, where load cycling is produced when the product is being subjected to varying temperatures. Many electronic components are designed with flexible leads to reduce the temperature effects of thermal fatigue. There are two types of fatigue: high cycle fatigue and low cycle fatigue. *High cycle fatigue* occurs when the thermal load is low, and the strain is in the elastic region, with reversible strain deformation. The number of cycles required is between 10,000 and 100,000. *Low cycle fatigue* occurs with high loads and the strain cycle is in the plastic region, with deformation occurring since the solder joint does not return to its original geometry. This is developed in less than 10,000 thermal cycles.

2. Creep: Creep is the result of continuous or repeated stress over time causing plastic (unrecoverable) deformation. This causes the joints to have increased elongation and reduced cross sectional areas. As a result, there might be contact resistance problems over time. Creep strain is both stress and temperature dependent, and begins with temperature varying at 35-75% of alloy melting temperature (based on the Kelvin temperature scale).

3. Impact or mechanical shock: This occurs when force or displacement is rapidly applied. The resulting stress deformation is much larger than if the force was applied gradually. This type of behavior is usually simulated by drop tests. Such tests would consist of dropping the product from a height of one meter onto a concrete floor. Solder joints rarely fail this test, and therefore this type of failure was not part of our reliability testing for lead-free SMT (Surface Mount Technology).

4. Reforming of Inter-metallic boundaries: Temperature cycling would cause migration of certain metals inside the alloy matrix, and therefore would affect some of the mechanical and electrical properties of the solder joints. This behavior is best investigated with cross-sectioning, although that was not performed during Phase I.

3.3.2 Temperature Cycling Profile

The thermal profile for temperature cycling lead-free solder joints was selected based on the following parameters.

- **Maximum temperature**: 100 degrees Celsius.
- **Minimum temperature**: 0 degrees Celsius.
- **Temperature ramp rates:** This is the rate of temperature change between the minimum and maximum temperature levels. The fastest possible rate (10 degrees C per minute) was selected to increase the effects of low cycle fatigue and creep.
- **Dwell times**: The dwell time at high and low temperatures was selected to be 20 minutes. This is the shortest time for the solder joint system to stabilize prior to reversing the temperature.

- **Number of cycles**: It was decided to visually inspect the joints for cracks every 200 hours of thermal cycling and to perform the pull test after 2,000 thermal cycles.

3.4 Pull Test Methodology

A major issue in developing the pull testing approach was how to develop a proper test fixture and method of pulling (straight and/or shear pulls) since no systematic method was found in the literature. A fixture was developed at UMass Lowell to lock in the test vehicles that allowed the pull instrument to align with the pulling head. The pulling instrument was a set of medical tweezers, which was modified for this test and attached to an Instron machine. The pull rate was set at 0.01 inches per minute to favor a solder joint failure, rather than a pad pull or lead break. Several pulls were made for each component, including the minimum solder joint break point, as well as the maximum pull at any point on the solder joint system (this maximum pull included pad lifts and broken leads). Only SO14 palladium components were included in the pull tests. Lessons learned during the pull tests included:

Angle: It was best to have a 45 degree pull as opposed to straight pulls. This approach resulted in both straight and shear pull forces.

Pad Fracture: Care needed to be exercised in monitoring the element(s) that separated. It was important not to confuse pad pulls or lead breakage with solder fracture, and to only record pull values when it was clear that only the solder pad fractured.

Recorded Values: It was desirable to pull all of the leads in a component so that a profile of the pull distribution was shown. The minimum value of the various pulls should be recorded, instead of the average value.

3.5 Pull Tests Result Summary

Solder joints were visually inspected every 200 cycles during the 2,000 total thermal cycle test, and no joint separations were observed. The statistical analysis of the maximum value pull tests before and after thermal cycling indicated that only the solder material was significant. All other factors did not influence the value of the pull tests. The pull strength of the different solder alloys remained essentially the same, and was much higher than the tin/lead baseline. Only the tin/lead pull strength increased after thermal cycling, due to changes in the inter-metallic composition of the copper migrating through the alloy towards the components.

The pull strength of the different solder alloys increased significantly, probably due to the fact that many of the pulls included those due to pad lifts, which tended to increase in value. This is probably due to better curing of the pad adhesion. Only the tin/bismuth solder did not increase in value, due to joint fractures. The temperature cycling did in fact relieve the creep strain on the joints, since the melting temperature of the tin/bismuth (138 degrees C) was close to the thermal cycling maximum temperature (100 degrees C). The statistical analysis indicated a slight (7%) effect of the surface finish, mostly due to the fact that the pad pulls influenced this analysis.

3.6 Conclusion

The Phase I research showed that it was possible to obtain a lead-free soldering process that exhibited a better reliability profile than that of the baseline tin/lead soldering. The selection of the material and processing parameters were very important to the defect-free visual performance of the lead-free soldering. For reliability performance, as expressed by thermal cycling, the tin/silver alloys were shown to be stronger than the tin/lead baseline and performed equally well after 2,000 thermal cycles. For subsequent phases of research, the decision was made to focus on SAC alloys, the inter-metallic structure of the alloys, additional printed circuit board surface finishes, and a ramp to peak thermal profile for reflow processes. [13]

4.0 PHASE II RESEARCH EFFORTS

4.1 Overview

Phase II research was conducted from 2002 through 2004, and included an examination of various solder alloy combinations and reflow profiles for the manufacture of lead-free electronic assemblies. The key contributors for the Phase II research efforts included Dr. Sammy Shina from the Department of Mechanical Engineering at the University of Massachusetts Lowell, Karen Walters from Skyworks, Marie Kistler from Air Products and Chemicals, Inc., Mark Quealy from Schneider Electric, David Pinsky from Raytheon Corporation, Richard McCann and Al Grusby from Analog Devices, Richard Anderson, Helena Pasquito, and George Wilkish from M-A/COM Tyco Electronics, Don Abbott from Texas Instruments, and Liz Harriman and Todd MacFadden from the Toxics Use Reduction Institute. This summary draws heavily from previous Phase II reports, including "A Comparative Analysis of Lead Free Materials and Processes Using Design of Experiments Techniques" by Shina, et al, published by SMTA in 2003. [15], and "Testing Results for Lead-free PWB's by the Massachusetts Lead-free Electronics Research Consortium", by Anderson et al presented at the IEEE International Symposium on Electronics and Environment in May, 2003. [16]

4.2 Experimental Design

A Design of Experiments matrix was selected by the Consortium members based on their collective experience and the available resources and materials. The factors and levels selected were as follows:

1. Printed circuit boards finishes:
   1) Solder Mask Over Bare Copper with Hot Air Solder Leveling (SMOBC/HASL)
   2) Matte Finish Tin (Sn) Electroplate
   3) Immersion Silver (Ag)
   4) Organic Solder Preservative (OSP)
   5) Electroless Nickel Immersion Gold (ENIG)

2. Reflow Atmospheres:
   1) Air
   2) Nitrogen, supplied by Air Products and Chemicals and containing 50 and 5,000 ppm oxygen

3. Solder Pastes: The solder pastes all had the same alloy composition—95.5Sn-3.8 Ag-0.7Cu—and were provided from three different suppliers (A, B and C). All solder pastes incorporated no-clean fluxes.

4. Component Lead Finishes:
   1) Matte Tin Plating
   2) SAC

3) Nickel/Palladium/Gold
4) Nickel/Gold

4.2.1 Test Vehicles

The test vehicle used for this phase of research was a 6" wide x 9" long test vehicle (printed circuit board), shown in the pull test fixture (see Figure 4.1). A total of 98 test vehicles were assembled and tested. The test vehicles were divided as follows:

1. 60 test vehicles: This consisted of two sets of 30 test vehicles to harness the full factorial experiment of five finishes, three solder suppliers and two reflow oven atmospheres (5 x 3 x 2 = 30). The full factorial experiment is shown in Table 4.1.

2. 10 test vehicles: This consisted of two sets of five test vehicles soldered with a leaded solder from supplier B to act as a baseline comparison to unleaded solder.

3. 8 test vehicles: This consisted of two sets of four test vehicles to test out a more concentrated percentage of nitrogen (50 ppm oxygen versus 5,000 ppm oxygen).

4. 20 test vehicles: This consisted of two sets of ten test vehicles, to compare the results of leaded and unleaded components versus leaded and unleaded solders, while using all five test vehicles finishes, an air soldering environment and solder supplier B. This set was tested to demonstrate whether it is possible to exchange unleaded components with leaded components within different soldering environments.

4.2.2 Components

The baseline tin/lead solder test vehicles were built with components that had a tin/lead component finish and the lead-free test boards were assembled with components that had lead-free finishes. The lead-free passive chips were tin-plated and the lead-free integrated circuit devices were plated with matte tin plating, SAC, nickel/palladium/gold, or nickel/gold. Components were donated from participating Consortium companies. Each test vehicle included the following components:

1. Standard surface mount technology (SMT) resistor and capacitor parts (401 and 402 styles)
2. A set each of 0.030 and 0.014 inch vias
3. 3 Quad Flat Package (QFP 176) high-density interconnection (HDI) package, one containing daisy chain terminations
4. 2 Ball Grid Array (BGA) types, 35 and 45 mm
5. 3 Small Outline Integrated Circuit (SOIC 20) packages, one containing daisy chain terminations
6. 3 special IC's used in wireless applications

The following table provides the surface finish, solder paste, and reflow atmosphere used for the 30 test vehicles in the full factorial design.

Table 4.1: ***Lead Free Full Factorial Solder Test Plan***

Experiment Number	Surface Finish	Solder paste	Reflow Atmosphere
1	SMOBC/HASL	"A"	Air
2	SMOBC/HASL	"A"	Nitrogen
3	SMOBC/HASL	"B"	Air
4	SMOBC/HASL	"B"	Nitrogen
5	SMOBC/HASL	"C"	Air
6	SMOBC/HASL	"C"	Nitrogen
7	OSP	"A"	Air
8	OSP	"A"	Air
9	OSP	"B"	Nitrogen
10	OSP	"B"	Air
11	OSP	"C"	Nitrogen
12	OSP	"C"	Air
13	ENIG	"A"	Nitrogen
14	ENIG	"A"	Air
15	ENIG	"B"	Air
16	ENIG	"B"	Nitrogen
17	ENIG	"C"	Air
18	ENIG	"C"	Nitrogen
19	Matte Sn	"A"	Air
20	Matte Sn	"A"	Nitrogen
21	Matte Sn	"B"	Air
22	Matte Sn	"B"	Air
23	Matte Sn	"C"	Nitrogen
24	Matte Sn	"C"	Air
25	Imm. Ag	"A"	Nitrogen
26	Imm. Ag	"A"	Air
27	Imm. Ag	"B"	Nitrogen
28	Imm. Ag	"B"	Air
29	Imm. Ag	"C"	Air
30	Imm. Ag	"C"	Nitrogen

4.2.3 Experiment Layout

The test vehicle was designed at M/A-COM, and the design incorporated the daisy chain resistance test capabilities in some of the components. The test vehicles were fabricated by Sanmina-SCI with the five different printed circuit board surface finishes. The solder pastes were obtained from three separate vendors and a reflow profile was developed based on the manufacturers' product data sheets. The Phase I test vehicle is shown below in Figure 4.1.

Figure 4.1: **Phase II test vehicle mounted in pull test fixture.**

A reflow profile board was populated with parts and three K-probe thermocouples were attached to the surface. One thermocouple was attached at the leading edge of the test vehicle, one at the lead attach area of a large QFP and one near the trailing edge of the test vehicle. The thermocouples were connected to an industry standard data logger. The thermal readings were downloaded to the data collector software for comparison to the manufacturer recommended profiles. All three manufacturers recommended a "ramp to spike" curve for a reflow oven profile. Several passes through the reflow oven were performed to ensure consistent performance.

Solder paste prints were made using a 0.006 inch thick stainless steel laser cut, electropolished stencil. Ten percent aperture reductions were used on the fine pitch devices. The major difficulties encountered during the assembly process were with the stencil printing and component placement. Paste A had a tendency to adhere to the sides of the stencil openings. This resulted in scant prints on some of the fine pitch apertures. Paste B periodically clogged the stencil, and required cleaning after every four or five prints. Paste C performed as expected with little difficulty. All three pastes exhibited good tack or component holding qualities during and after placement.

The test vehicles were assembled at Schneider Electric on their assembly line consisting of an MPM AP-25 screen printer, Siemens S20 and F5 placement equipment, and a BTU Pyramax 98N Reflow Oven with air and nitrogen atmosphere capability. The reflow oven atmosphere was supplied by BTU International for this experiment. The Schneider plant maintained a relative humidity level between 35 and 40% during the assembly process.

4.3 Visual Analysis Results

After reflow, the test vehicles were packaged in Electrostatic Discharge (ESD) bags and taken to the M/A-COM facility where two University of Massachusetts Lowell students visually inspected the solder joints. The inspection was based on training received by a certified IPC inspector/trainer. The inspection criteria were established for the following defect categories: Cold Solder joints, Non-wetting, Solder Balls, Dewetting, Bridging, Pinholes, Shiny Appearance, Smooth Appearance, Flux Residue, and Total Defects. X-ray radiography of the BGA solder joints was also performed. Initial inspection data was tabulated and statistically analyzed by University of Massachusetts Lowell and Air Product personnel. The observed defects were photographed and recorded into a spreadsheet. Statistical analyses were performed using Minitab software.

Table 4.2: ***Statistical Analysis – Total Visual Defects - ANOVA for 0.35 Power Transformed (Total Defect Data)***

Source	Degrees of Freedom (DF)	Sum of Squares (SS)	Mean Square (MS)	F Value	P Value
Finish	4	44.7	11.2	7.33	0.0003
Solder	2	79	39.5	25.91	<0.0001
Atmosphere	1	132.4	132.4	86.88	<0.0001
Finish and Solder Interaction	8	16.0	2.0	1.32	0.273
Finish and Atmosphere Interaction	4	15.3	3.8	2.51	0.063
Solder and Atmosphere Interaction	2	54.3	27.2	17.83	<0.0001

The Analysis of Variance (ANOVA) results can be used for hypothesis testing. The null hypothesis used for this research is that the solder defect values for different factor/level combinations within the experimental design are the same for each combination. The alternative hypothesis is that the expected solder defect values for different factor/level combinations within the experimental design are not the same. A P-value is a measure of how much evidence we have against the null hypotheses about the population. P-values represent the probability of making a Type 1 error, or rejecting the null hypothesis when it is true. The smaller the P-value is, then the smaller is the probability that you would be making a mistake by rejecting the null hypothesis. For the purposes of this research, if the P-value is 0.05 or less, then the solder defect results were considered to be significantly different and likely to support the alternative hypothesis.

As seen in the table above, the ANOVA is significant for the overall experiment and for the variables highlighted with probabilities (P-values) less than 0.05.

The statistical analysis indicated the following results:

1. The solder defect levels for the SMOBC/HASL surface finish significantly differs from all other finishes. No other finishes were found to be statistically different from one another at the 0.05 probability level.

2. The solder defect levels for all solder pastes were found to differ significantly from all other pastes. Solder paste supplier B Pb-Free performed the best.

3. The test vehicles assembled in a nitrogen reflow environment performed significantly better (less solder defects) than an air reflow environment.

4. The Supplier A Pb-Free and Air combination was significantly worse than all other combinations. The Supplier C Pb-Free and Air combination was significantly worse than all other remaining combinations. The next four lowest combinations: 1) Supplier B Pb-Free with Air, 2) Supplier B Pb-Free with Nitrogen, 3) Supplier A Pb-Free with Nitrogen, and Supplier C Pb-Free with Nitrogen, could not be statistically differentiated within the limitations of the study.

5. For solder paste B, there was no significant difference between the use of air or nitrogen reflow environment.

6. There were not enough data points to analyze the differences in visual defect data between the two levels of nitrogen in the experiment (50 ppm versus 5000 ppm oxygen).

7. There were not enough data to analyze the differences in visual defects between unleaded and leaded components using lead and unleaded solders from the same solder supplier.

4.4 Pull Test Analysis Results

The test methodology consisted of using an Instron pull test machine to pull the leads of a component at different positions and record the maximum pull force. The pull tests were analyzed separately for each type of component because of the differences in pad size and component finish.

For the QFP (nickel/palladium/gold) component leads, six leads were pulled, and for the SOIC 20 (nickel/palladium/gold) and the SOIC 16 (tin finish) component leads, four leads were pulled.

The process of pulling the leads was performed as follows:

1. The test vehicle was loaded at a 45 degree angle to the Instron machine and was anchored with six screws on a specially designed hold down fixture.

2. The leads adjacent to the ones that were pulled were removed (clipped) to facilitate pulling of the target leads.

3. The leads that were pulled were tied with a wire loop right through the IC's leads. Music wire was used for QFP components, and fishing line (24-pound test) was used for SOIC components.

4. A new loop was made for each component pulled.

5. The pull rate was 1 inch per minute, and the peak pull force was recorded.

6. The fractures were inspected and the failure mode for each pull was documented.

Two test vehicles were unable to be pulled because of improper reflow in one case and severe bending in the other case.

4.4.1 QFP-176 and SOIC-20 Pull Test Results

The leads of the QFP-176 and SOIC-20 components that were pulled had a nickel/palladium/gold finish. Six pulls were made for each of the 30 QFPs in the full factorial experiment, for a total of 168 pulls; two components were not included in the pull effort because of problems during soldering. Four pulls were made for each of the 30 SOICs for a total of 112 pulls. The ANOVA analysis for the QFPs is shown in Table 4.3 and for the SOICs in Table 4.4.

Table 4.3: ***Statistical Analysis – QFP Pull Test (6 pulls per IC)***

Source	Degrees of Freedom (DF)	Sum of Squares (SS)	Mean Square (MS)	F value	P value
Surface	4	5.36	1.34	5.00	0.001
Solder	2	1.70	0.85	3.17	0.045
Atmosphere	1	4.32	4.32	16.10	0.000
Surface*Solder	8	18.6	2.33	8.68	0.000
Surface*Atmosphere	4	1.04	0.26	0.97	0.428
Solder *Atmosphere	2	3.00	1.50	5.57	0.005
Error	146	39.1	0.26	N/A	N/A
Total	167	73.7	N/A	N/A	N/A

Table 4.4: ***Statistical Analysis – SOIC Pull Test (4 pulls per IC)***

Source	Degrees of Freedom (DF)	Sum of Squares (SS)	Mean Square (MS)	F value	P value
Surface	4	77.00	19.30	7.35	0.000
Solder	2	17.72	8.860	3.38	0.038
Atmosphere	1	1.758	1.758	0.67	0.415
Surface*Solder	8	14.25	1.782	0.68	0.707
Surface*Atmosphere	4	28.72	7.180	2.74	0.033
Solder *Atmosphere	2	9.970	4.985	1.90	0.155
Error	90	235.6	2.618	N/A	N/A
Total	111	392.8	N/A	N/A	N/A

4.4.2 Factorial Experiment Analysis for QFP and SOIC Pulls

The results of the pull test data is summarized below:

1. Since all leads had a nickel/palladium/gold finish, these conclusions were only applicable to this component surface finish material.

2. The pull force in the SOIC component was significantly higher than that of the QFP component due to the large solder surface area in the component pads.

3. The surface finish has a significant effect on the pull test of the leads. Of the five finishes examined, the analysis showed that the ENIG surface finish had significantly lower pull strength than the other finishes for both types of components. The OSP surface finish had significantly higher pull strength for the QFP components, and the SMOBC/HASL surface finish had significantly higher pull strength for the SOIC components.

4. The solder supplier was not an important factor in the pull tests for the two component types. Supplier B pull strength was slightly higher for the QFP-176 and significantly higher for the SOIC-20 component.

5. The pull strength for the nitrogen reflow environment was significantly higher than air reflow environments for the QFP-176 component, but not significant for the SOIC 20 component.

4.5 Comparison of Unleaded Solder With Leaded Solder Pull Tests

For each of the five surface finishes, a test vehicle was reflowed with the leaded solder from supplier B in an air reflow oven environment, which was used as the baseline for comparing the pull test results for the lead-free test vehicles. Figures 4.2 and 4.3 show the comparisons for QFP and SOIC respectively. All components included in the pull testing had the nickel/palladium/gold component finish.

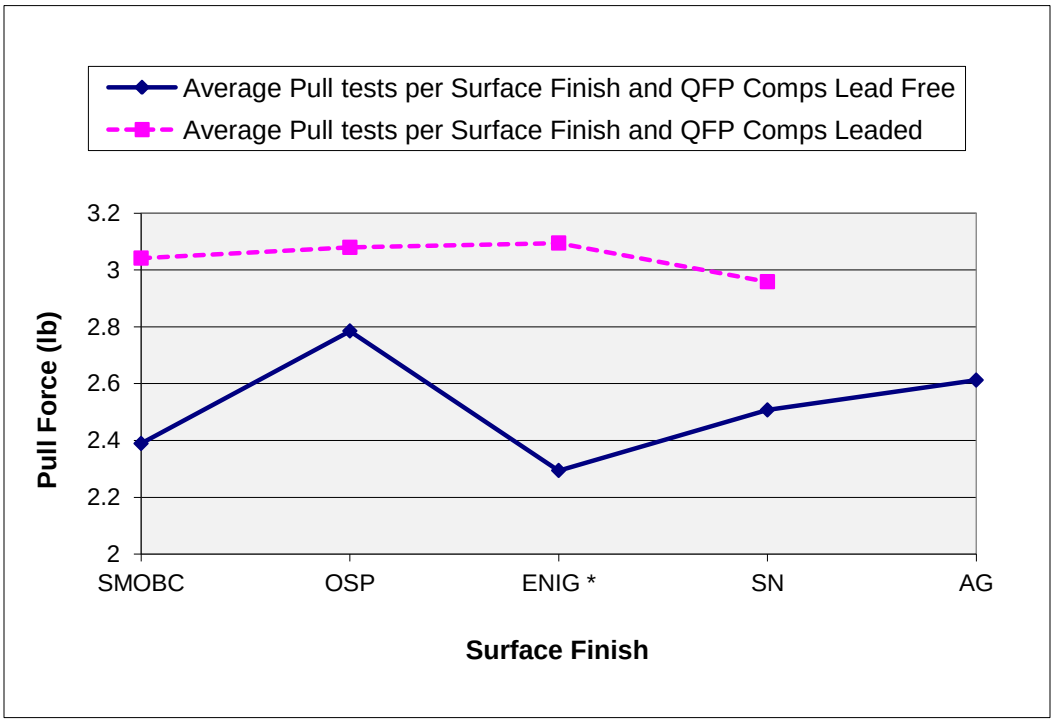

Figure 4.2. **Comparison of unleaded versus leaded solder and QFP components.**

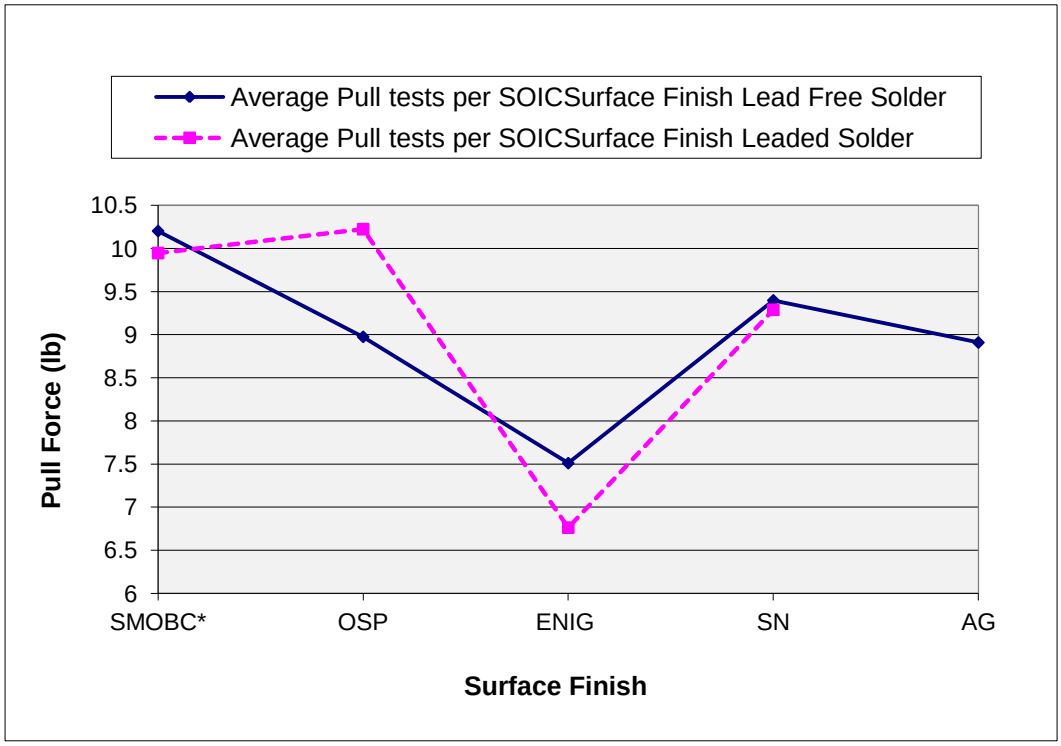

Figure 4.3. **Comparison of unleaded and leaded solder - solder per PCB surface finish and SOIC20 components.**

Since the nitrogen reflow oven environment was a significant factor for the QFP-176 component, only air soldered test vehicles from each finish (three test vehicles for each of five board finishes) were used in the comparison for the QFP component. For the SOIC-20 component, all test vehicles (six test vehicles for each of the five board surface finishes) were used in the comparison to the leaded solder baseline. The comparisons were made using a multiple-range test for means. Unfortunately, the baseline test vehicle for immersion silver (Ag) finish with leaded solder was not available. The analysis had to be performed separately for QFP-176 and SOIC-20 because of the higher pull force for the SOIC components. The following results were observed:

1. For all the Supplier B provided leaded solder pastes that were used as baseline and air reflowed; the QFP-176 lead pull strength showed no significance due to test vehicle surface finish. The SOIC-20 component lead pull strength showed that ENIG was the only significant (lower) pull force.

2. Unleaded and leaded pull tests showed no significant differences, if the same solder supplier provided the solder paste, except for the QFP component with the ENIG surface finish and the SOIC component with the SMOBC surface finish. This might indicate that other factors such as solder paste formulation may have played a role in making a significant difference between leaded and unleaded solder, more so in smaller footprint components such as QFP.

3. When comparing leaded solder supplier B with all three unleaded solder suppliers, some significant differences arise. For the immersion silver (Ag) surface finish, the comparison was not possible since the baseline data were not recorded because of manufacturing problems with the sample test vehicles.

An additional test was conducted to determine the compatibility of lead/lead-free solder materials with lead/lead-free component finishes. This test was performed for tin plated SOIC 16 components, to determine whether leaded and/or unleaded solder and/or components with tin plating finish could be used for different types of printed circuit board surface finish. This would enable component customers to achieve forward and backward compatibility as the industry transitions to lead-free technology. Seven combinations (21 pairs) of solders and component-finishes were tested. There were no significant differences in the results.

4.6 Conclusions

This phase of the research shows the effects of atmosphere, paste selection, and printed circuit board surface finish on visual appearance defects and an initial reliability assessment of lead-free soldering. The nitrogen reflow oven environment and solder paste B yielded the fewest visual defects and the SMOBC/HASL surface finish resulted in significantly more visual defects.

For pull testing, this research established conclusions for the following three major areas:

1. The selection of materials and process affected the pull strength of the lead-free solder joints for the QFP and SOIC components tested when using components with a nickel/palladium/gold finish.

- The pull forces were dependent on the footprint of the components used; consequently, pull forces in the SOIC component were significantly higher than in the QFP component.

- The test vehicle surface finish has a significant effect on the pull test of the leads. Of the five printed circuit board finishes examined, the ENIG surface finish yielded significantly lower results than the other finishes for both types of components included in the pull test. The OSP surface finish had significantly higher pull strength in QFP components and the SMOBC/HASL pull strength was significantly higher for SOIC components.

- The solder suppliers were not statistically significant in the pull tests for both types of components included in the test. Supplier B had slightly higher pull values for the QFP component and significantly higher values for the SOIC component.

- The pull strength value for the nitrogen reflow atmosphere was significantly higher than air reflow for the QFP components, but not significant for SOIC components.

2. The comparison of the unleaded solder pulls to leaded solder pulls in QFP and SOIC, using components with nickel/palladium/gold finish was difficult since the baseline leaded test vehicles were assembled with a single process. The test vehicles were soldered in an air reflow environment with leaded solder from supplier B, where the silver surface finish baseline was not available. The data indicated that the difference is not significant in most cases when using the same solder supplier (B) for unleaded and leaded solders.

3. The interchangeability of leaded and unleaded components and solders in SOIC and tin plated components pull tests is an important issue. Electronic component suppliers and customers are concerned about keeping a dual set of materials for different markets around the world as the technology transitions from leaded to lead-free soldering. The results indicated that for the set of seven conditions analyzed, with 21 pair-wise tests, there was no significant difference in the pull test results. Note that the baseline condition of leaded solders and component finishes, and the ultimate condition of lead-free solders and component-finishes, were not tested. [15]

5.0 PHASE III RESEARCH EFFORTS

5.1 Overview

Phase III efforts were conducted between 2004 and 2007. The objective of Phase III testing was to focus on manufacturing implementation issues by simulating an actual production board for parameters such as board layers, board size, component geometry, and component density. The Phase III test vehicle was a twenty-layer board with components on both sides, populated with 1,750 components. Thirty-six test vehicles were built and inspected to IPC 610 D standards by Benchmark Electronics during 2005. The test vehicles underwent thermal cycling at Raytheon Reliability Labs test facilities and Highly Accelerated Lifetime Testing (HALT) at Teradyne test facilities. Pull testing was conducted at the University of Massachusetts Lowell. This summary draws heavily from previous Phase III reports including "Visual and Reliability Testing Results of Surface Mounted Lead Free Soldering Materials and Processes in a Simulated Production Environment" by Morose et al presented at the APEX 2006 conference. [17]

The following individuals provided key contributions to the Phase III research efforts:

- The U.S. EPA for providing funds for Phase III lead-free research under order number 4W-1362-NAEX.
- The Toxics Use Reduction Institute for project management and statistical analysis.
- The University of Massachusetts Lowell for pull testing and statistical analysis.
- StenTech and Yankee Soldering for providing stencil technology and expertise to the Consortium.
- Dynamic Details Inc. for providing the test vehicles and circuit board design expertise for Phase III.
- Benchmark Electronics, Skyworks Solutions, M/A-COM, Textron, Teradyne, Raytheon, Texas Instruments, and American Power Conversion for providing components for the test vehicles.
- Niton LLC for providing a portable XRF analyzer for verification and non-destructive analysis of lead content in the various materials included in the experiment.
- Teradyne for providing HALT test facilities and accelerated testing expertise.
- Raytheon Company Reliability group for providing testing expertise and equipment for thermal cycling of the test vehicles.

5.2 Experimental Design

Phase III testing efforts focused on examining the manufacturing issues of implementing lead-free electronics assembly for printed circuit boards more closely resembling actual production boards. Whereas previous research phases utilized experimental test vehicles that were single layer, single sided, small footprint, and sparsely populated with only SMT components, the test vehicle for Phase III

was designed to better simulate actual production boards commonly used in industry. The Phase III board had a variety of component types and finishes, as well as some active circuitry that could be tested for electrical performance. The object of Phase III was to compare the solder joint integrity and circuit performance between lead and lead-free electronics assembly for production scale boards. The primary metrics for this comparison were the following:

- Defects per unit (DPU) as identified during the visual inspection process, and
- Peak pull strength as measured during pull testing.

The Phase III test vehicle had a large footprint of 16"by 18". As mentioned above, it was comprised of 20 layers and was densely populated with components on both sides. Phase III included 36 printed circuit boards. Each test vehicle contained 1,713 surface mount technology (SMT) type components and 53 through hole technology (THT) type components, for a total of approximately 62,000 components.

Prior results of Consortium testing efforts, as well as other published research, was incorporated into the material and process selection for Phase III lead-free testing. New Consortium members were added to provide resources and background to volume production application of lead-free electronic assembly. These companies provided valuable knowledge and material contribution of mass market volume applications.

5.2.1 Factors and Levels of the Lead-free Experiment

The following factors were selected based on results of Phase I and II research efforts, as well as the collective experience of the Consortium members: three surface finishes, two lead-free solder suppliers ("A" and "B"), and two types of laminate materials ("Y" and "Z"). The vendor name and product model numbers were known to the Consortium members, but not disclosed in publicly available documentation. The three surface finishes selected were electroless nickel immersion gold (ENIG), immersion silver, and organic solderability preservatives (OSP). The lead-free solder from both suppliers used the SAC 305 alloy and no-clean flux. Other factors, such as solder reflow profile (as recommended by the supplier) and atmosphere (air), were fixed based on Consortium member consensus. Each test vehicle had at least two reflows during assembly, one for the top side of the test vehicle and another for the bottom side of the test vehicle. Two test vehicles were built for each of the lead-free experiments listed in Table 5.1, for a total of 24 lead-free test vehicles.

Table 5.1: ***Phase III Lead Free Solder Test Plan***

Experiment #	Surface Finish	Solder Paste	Laminate
1	(1) Imm Ag	LF "A"	"Y"
2	(1) Imm Ag	LF "A"	"Z"
3	(1) Imm Ag	LF "B"	"Y"
4	(1) Imm Ag	LF "B"	"Z"
5	(2) OSP	LF "A"	"Y"
6	(2) OSP	LF "A"	"Z"
7	(2) OSP	LF "B"	"Y"
8	(2) OSP	LF "B"	"Z"
9	(3) ENIG	LF "A"	"Y"
10	(3) ENIG	LF "A"	"Z"
11	(3) ENIG	LF "B"	"Y"
12	(3) ENIG	LF "B"	"Z"

5.2.2 Baseline Leaded Solder Experiments

To reduce the number of iterations in the lead baseline experiments, only one laminate material was used with three different surface finishes and two different leaded solder suppliers. Two test vehicles were built for each of the leaded experiments listed in Table 5.2, for a total of 12 leaded test vehicles.

Table 5.2: ***Leaded Solder Test Plan***

Experiment #	Surface Finish	Leaded Solder Paste	Laminate
1	(1) Imm Ag	TL "A"	"Z"
2	(1) Imm Ag	TL "B"	"Z"
3	(2) OSP	TL "A"	"Z"
4	(2) OSP	TL "B"	"Z"
5	(3) ENIG	TL "A"	"Z"
6	(3) ENIG	TL "B"	"Z"

5.2.3 Components

Surface mount and through-hole technology components were used for the Phase III test vehicle. Component types include ball grid arrays (BGAs), small outline integrated circuits (SOIC), connectors, resistors, capacitors, relays, inductors, and quad flat packs (QFPs). A variety of component finishes were included, including nickel/palladium/gold, tin, tin/lead, gold, nickel/gold, tin/nickel, palladium/silver,

tin/copper, SAC, tin/bismuth, and matte tin. Some components were available in daisy chain configurations for electrical testing.

5.3 Assembly Process

The test vehicle was designed by Benchmark Electronics, and the raw printed circuit boards were manufactured by Dynamic Details Inc. Two stencils (one for the top and one for the bottom of the printed circuit board) were manufactured by Stentech and were 6-mil thick electropolished laser cut stainless steel. There was a step-down to 5 mils on both stencils to accommodate the microBGAs.

A ten percent (10%) standard reduction was used for the apertures on the top stencil. The apertures for the bottom stencil included:

1) For leaded devices, there was a 10% expansion in length for both directions, and a 1 to 1 ratio for width.
2) For fine pitch devices, aperture ratio was based on pad size.
3) For discrete components there was a 10% increase in length on the termination side only, and a 1 to 1 ratio for the width.

The same stencils were used for both the lead-free and tin/lead test vehicles. The discrete components were divided into four groups, each group containing both resistors and capacitors. Each group had different aperture styles, including radial aperture, home plate, king's crown, or standard aperture.

Assembly of the Phase III test vehicles was conducted at Benchmark Electronics. The equipment used for the SMT components included a DEK Horizon 265 screen printer, a Universal 4791 high speed placement machine, and a Vitronics XPM reflow oven with 10 heating zones and 3 cooling zones. For the THT components, Premier Rework machines were used. The solder pot temperature was 260^{o} C for the tin/lead test vehicles and 280^{o} C for the lead-free test vehicles. The automatic optical inspection was conducted using an Omron VT-WIN inspection system. Visual inspectors then conducted 100% visual tests on all solder joints for each of the Phase III test vehicles. The test vehicles were then available for Consortium members to conduct further visual inspection and electrical testing of their components.

Upon completion of visual inspection and electrical testing, the test vehicles then underwent reliability testing. The Phase III test vehicles were divided evenly for the reliability testing. Half of the test vehicles underwent thermal cycling, and the other half underwent Highly Accelerated Life Testing (HALT testing). Pull tests were performed on the four spare test vehicles prior to thermal cycling, and on eighteen test vehicles after thermal cycling. The four spare boards were all lead-free test vehicles.

5.4 Interconnect Stress Test

Initially, all test vehicles were tested using a coupon for interconnect stress test (IST) to evaluate the higher temperature effects on the laminate materials. This test measures changes in resistance of plated through hole barrels and internal layer connections as the test coupon is subjected to thermal cycling. Thermal cycling is produced by applying an electrical DC current through the test coupons. Switching the

current on and off creates thermal cycles between ambient temperature and the desired maximum temperature.

To simulate a lead-free assembly environment, the IST preconditioning temperature was set at 260° C. To obtain a greater understanding of the effect of multiple heat excursions on the laminate material, half of the test coupons had three heat cycles during preconditioning and the other half of the test coupons had six heat cycles during preconditioning. The preconditioning temperature profile is shown in Figure 5.1.

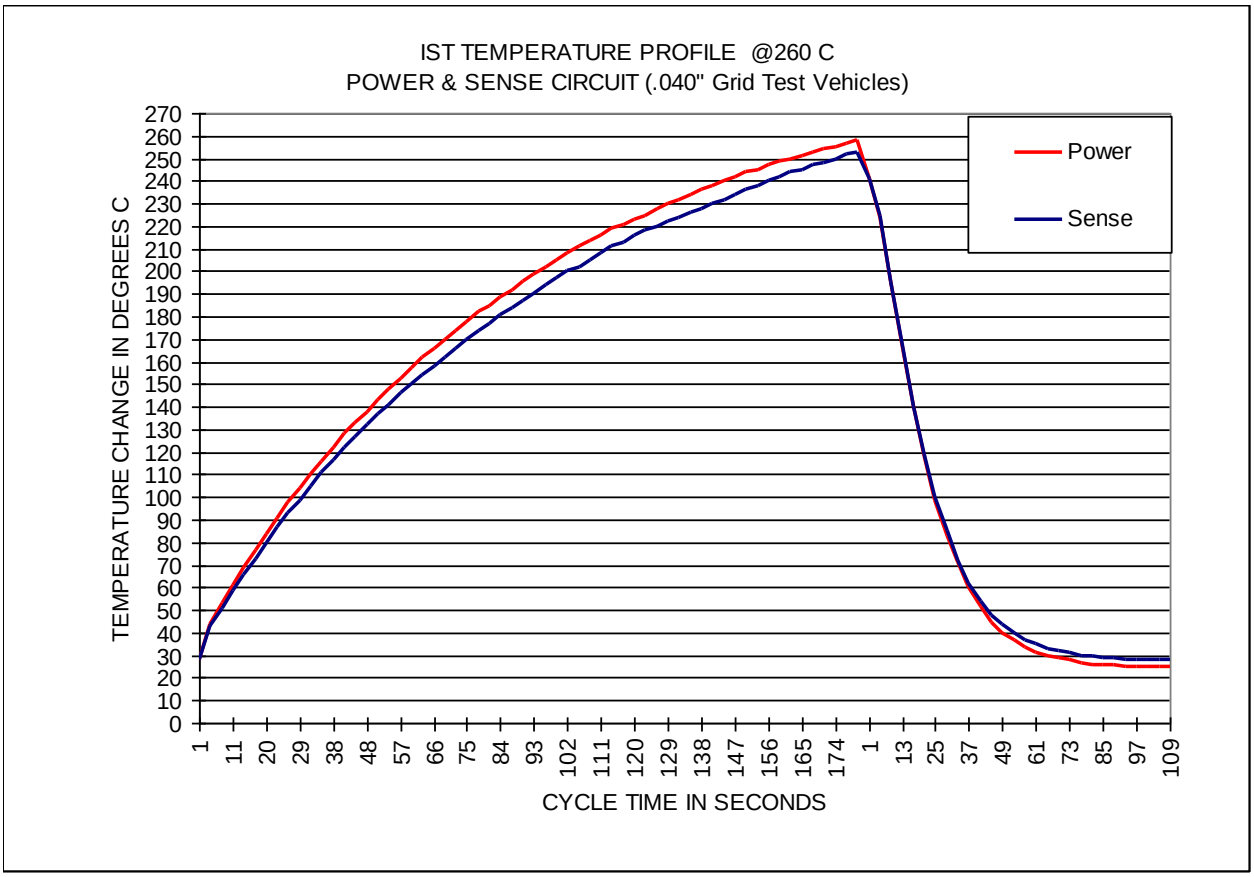

Figure 5.1: **IST preconditioning temperature profile.**

After the test coupons passed the preconditioning, they underwent IST cycling for up to 500 cycles. Each IST cycle lasted approximately 85 minutes and the temperature was cycled between ambient and 150° C for some tests, and between ambient and 190° C for other tests. The thermal profile for the 150° C IST cycling is shown in Figure 5.2.

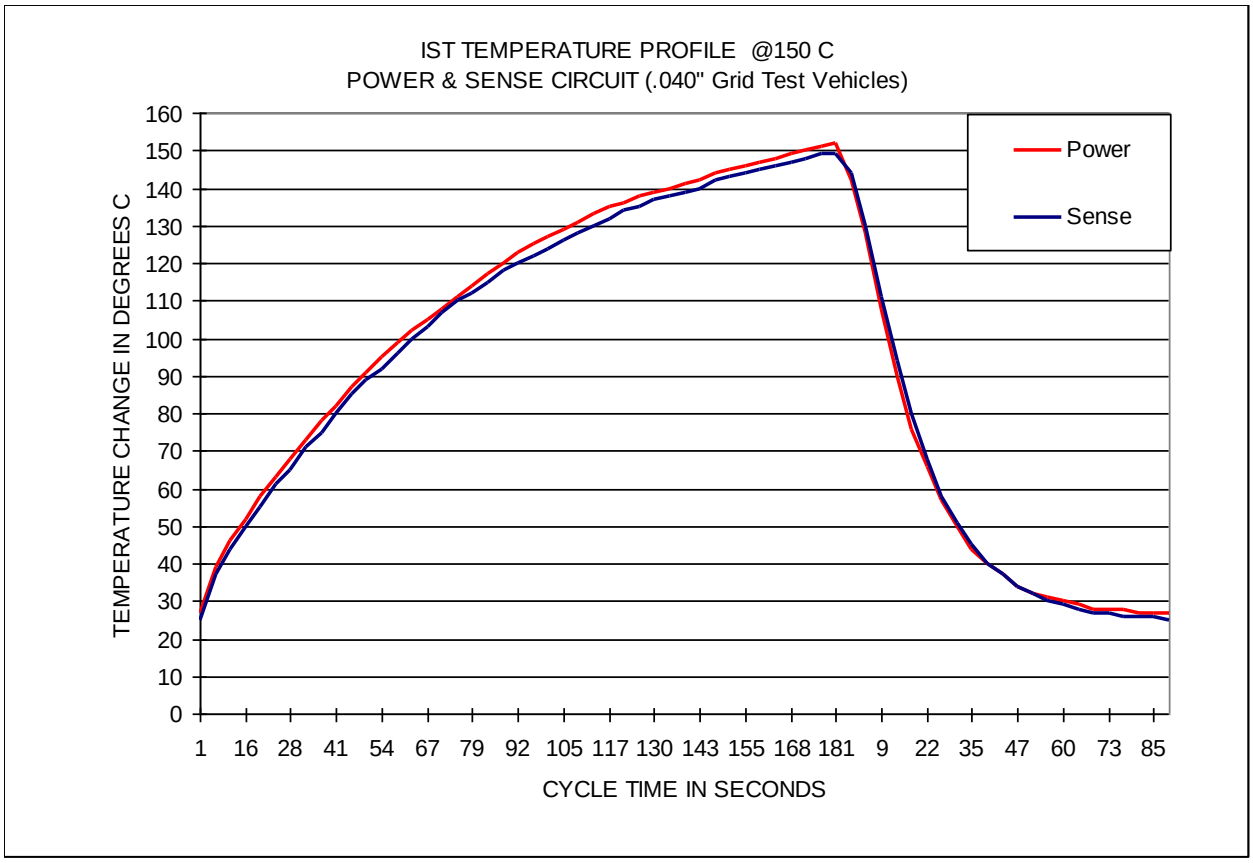

Figure 5.2. **IST cycle temperature profile.**

The number of cycles to failure was recorded for each test coupon. The IST 150^{o} C results are shown in Table 5.3. The results revealed a bimodal distribution in that the test coupons either failed early in the thermal cycling, or they made it all the way through the preconditioning and IST cycles without failure. A possible cause for the bimodal data could be defects in some test vehicles' holes, such as the presence of debris or insufficient plating of the high aspect ratio through holes.

Another interesting result is the high number of failures for the test coupons with OSP surface finishes, and the low number of failures for test coupons with ENIG and immersion silver surface finishes. Board surface finish is not expected to be a significant factor in IST results. The OSP coating was not applied before the IST testing. Therefore, the IST testing was done on bare copper in an air environment. The OSP failures could have been false failures caused by the formation of copper oxide at higher temperatures.

Table 5.3: *150^{o} C IST Results*

Material	Finish	Precondition Cycles	P/F	Cycle Failure Occurred	No. of IST Cycles Completed
A	ENIG	3x	P	No failure	500
A	OSP	3x	F	Cycle 3	3
A	Ag	3x	P	No failure	500
A	ENIG	6x	F	Cycle 5	5
A	OSP	6x	F	Cycle 5	5
A	Ag	6x	P	No failure	500
B	ENIG	3x	P	No failure	500
B	OSP	3x	F	Cycle 29	29
B	Ag	3x	P	No failure	500
B	ENIG	6x	P	No failure	500
B	OSP	6x	F	Cycle 1	1
B	Ag	6x	P	No failure	500

ANOVA analysis was not performed for the IST testing results because of the presence of significant confounding factors such as material damage and variations in coupon manufacture. The material damage can cause stress relief and increase IST cycles. However, some qualitative conclusions can be made based upon the results obtained. It appears that the majority of the material damage was induced by the tin/lead and lead-free preconditioning with one exception: the coupons with the HASL finish for the 190 ^{o}C microvia testing with no preconditioning. These coupons did not have significant material damage for all three coupons tested. Overall, the material damage in most cases seemed to provide stress relief capability and consequently increased the number of IST cycles before failure.

There were no failures during the actual preconditioning of the coupons. All of the failures identified occurred during the IST cycling independent of the preconditioning conducted beforehand. The coupons with the lead-free HASL surface finish did not have any failures before 500 IST cycles for all IST testing, however, the material damage for these coupons was higher than for any other type of coupon. The high Tg FR4 coupons with OSP finish had the most failures for the plated through hole testing at 150 ^{o}C, and the coupons with ENIG finish had the most failures for the microvia testing at 190 ^{o}C.

A completely successful IST would occur if there were no recorded failures before 500 IST cycles and the average maximum capacitance change was less than 5%. The coupon that came closest to this situation was the halogen-free laminate material coupon with OSP finish for the microvia testing at 190 ^{o}C.

There did not appear to be a major difference in the failure or material damage results between the coupons with tin/lead preconditioning as compared to the coupons with lead-free preconditioning. In

general, the laminate materials performed well during the IST testing, and the board surface finish was not considered to be a significant factor for IST failures.

5.5 Visual Inspection Results

After the Phase III test vehicles were assembled, they were visually inspected at Benchmark Electronics. Seven visual inspectors conducted 100% visual tests on all solder joints based on IPC inspection standard 610D. The results of the Automatic Optical Inspection were reviewed for false/true calls by the visual inspectors. The microscopes were set at 10x magnification, and inspections were conducted in accordance with Class 2 requirements. Each of the 36 test vehicles was inspected by two different visual inspectors.

Seventy potential defect and process indicator categories were used during this visual inspection, including non-wetting, pinholes, solder balls, solder bridging, and tombstoning. Table 5.4 reveals the actual defects and process indicators that were identified for both the tin/lead and lead-free test vehicles.

Table 5.4: ***Identified Defects and Process Indicators***

Description	Tin/Lead printed circuit boards	Lead-free printed circuit boards
209: Bent pin	Y	Y
261: Tombstone	Y	Y
602: Solder bridge	Y	Y
615/616: Non-wetting	Y	Y
626: Disturbed solder	Y	Y
713: Foreign matter	Y	Y
606: Pinholes, blowholes	Y	Y
613: Insufficient solder	Y	Y
672: Solder balls	Y	Y
205: Misregistration	Y	Y
270: Raised part	Y	Y
603: Solder splatter	Y	Y
612: Excess solder	Y	Y
620: Unsoldered lead	N	Y
701: Delamination	N	Y
770: Damaged pad	Y	Y

In total, 993 defects were identified during the visual inspection. This total includes 2 visual inspections for each of the 36 test vehicles. Table 5.5 shows grouping by component type (surface mount and through hole) for the defects found.

Table 5.5: ***Defects Identified During Visual Inspection***

Component Type	Lead-free 24 printed circuit boards (x2 inspections)	Tin/Lead 12 printed circuit boards (x2 inspections)	Totals
SMT	377	349	726
THT	246	21	267
Totals	623	370	993

For the SMT components, the defects per unit (component) rate was 0.5% for the lead-free test vehicles, and 0.8% for the tin/lead test vehicles. For the THT components, the defects per unit (component) rate was 19.3% for the lead-free test vehicles, and 3.3% for the tin/lead test vehicles.

The results of the visual inspection are described in the following three sections:

1. Design of experiment analysis 1: Lead-free printed circuit board visual defects
2. Design of experiment analysis 2: Tin/lead printed circuit board visual defects
3. Comparison of lead-free versus tin/lead printed circuit board visual defects

The null hypothesis is that there is no difference between the compared values. The alternative hypothesis is that there is a difference between the compared values. A 95% significance level was used for the visual inspection results. If the calculated probability was less than 0.05, then the null hypothesis was not rejected. If the calculated probability was greater than 0.05, then the null hypothesis was rejected, indicating that there was a difference between compared values.

5.5.1 Lead-free Printed Circuit Board Visual Defects

The mean defects per printed circuit board are provided in Figure 5.3. For the purposes of this research, we considered the results to be statistically significant if the Confidence Level was at least 95%, with a corresponding alpha risk of 5%. Therefore, if the P value is 0.05 or less, the results were considered significant. The mean defects per board for lead-free solder "A" was 10.83, and the mean defects per printed circuit board for lead-free solder "B" was 4.87. With a P value of 0.055, the difference between the performances of lead-free solders "A" and "B" is of borderline significance.

The mean defects per printed circuit board for laminate material "Y" was 10.83, and the mean defects per printed circuit board for laminate material "Z" was 4.87. With a P value of 0.055, the difference between the performance of laminate materials "Y" and "Z" is of borderline significance.

For the three board surface finishes, there was a P value of 0.298. Therefore, there is no statistical difference between the three surface finishes for the lead-free printed circuit board visual defects.

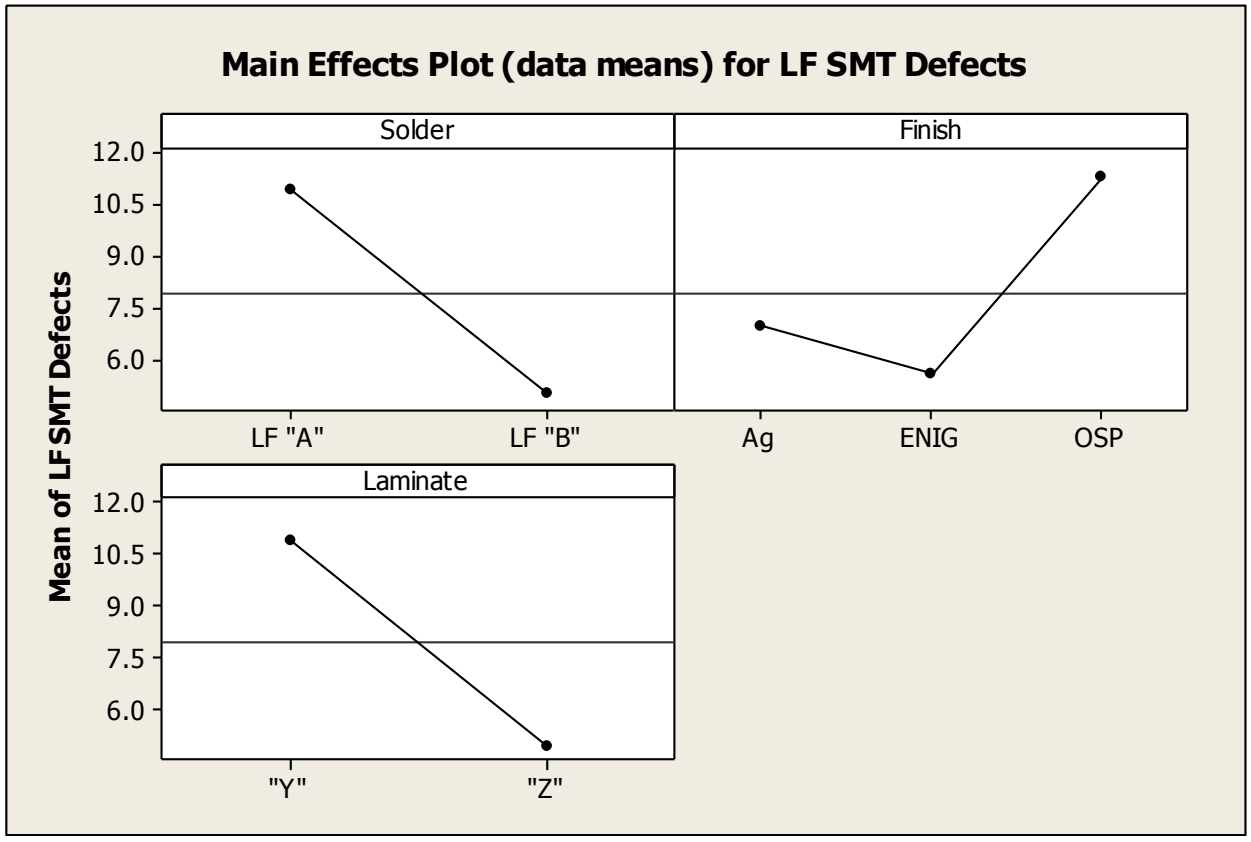

Figure 5.3. **Mean SMT defects per lead-free printed circuit board.**

From the interaction analysis, there was statistical significance only for the laminate and solder paste interaction. The interaction of lead-free solder "A" with laminate material "Y" had a mean defects per printed circuit board of 17.17, which was much higher than the other three lead-free solder and laminate combinations. The values of all the interactions can be seen in Figure 5.4.

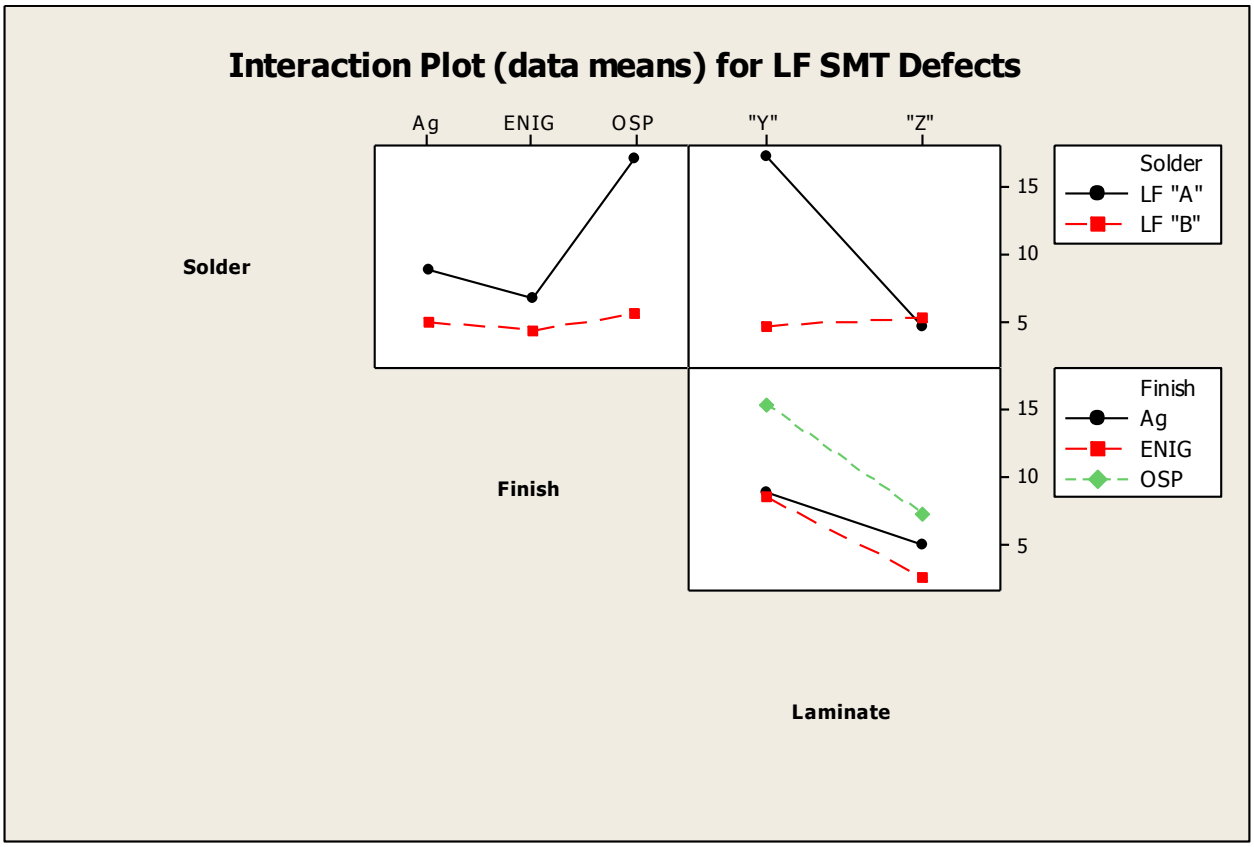

Figure 5.4. **Lead-free interaction effects.**

For the through hole technology (THT) components on the lead-free printed circuit boards, there was no statistical significance for any of the factors: laminate material, surface finish, or solder paste. There was also no statistical significance for interaction effects for the THT components.

5.5.2 Tin/Lead Printed Circuit Board Visual Defects

Figure 5.5 illustrates the mean defects per printed circuit board for the tin/lead printed circuit boards.

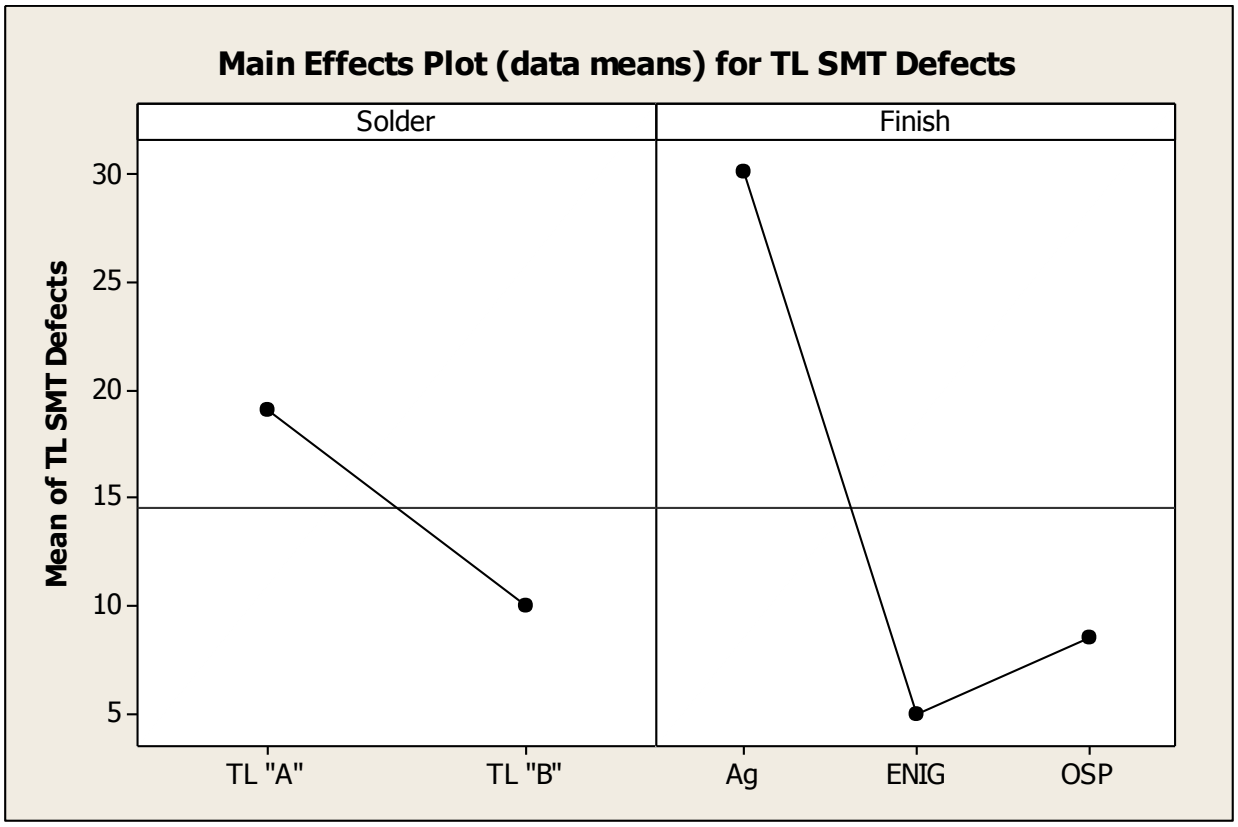

Figure 5.5. **Mean SMT defects per tin/lead printed circuit board.**

For the tin/lead printed circuit boards, there was no statistical difference for solder paste, surface finish, or interaction effects for SMT or THT components.

5.5.3 Comparison of Lead-free Versus Tin/Lead Printed Circuit Board Visual Defects

The mean for THT component visual defects per printed circuit board was 10.2 for lead-free boards, and 1.7 for tin/lead printed circuit boards. Because the probability is less than 0.05, there is a statistical difference between the means for lead-free and tin/lead printed circuit boards. Therefore, the tin/lead process has a lower rate of defects for THT components.

The mean for SMT component defects per printed circuit board was 7.9 for lead-free printed circuit boards, and 14.5 for tin/lead printed circuit boards. Because the probability is greater than 0.05, there is no statistical difference between the means for lead-free and tin/lead printed circuit boards. Therefore, the tin/lead and lead-free process were considered to have a similar rate of defects for SMT components.

5.5.4 Component Finish Visual Defects

There were ten different SMT component finishes used for the lead-free and tin/lead printed circuit boards. Table 5.6 provides the solder joint defect rate for each of the component finishes. The matte

tin (8.3%) and nickel/gold (18.7%) had the highest defect rates for the lead solder, and the nickel/gold (9.1%) and SAC (13.5%) had the highest defect rates for the lead-free solder. The defect rate provides a relative indication of the performance of each component finish. However, further statistical analysis was not conducted on the component finish defect results because: 1) there were many different component package/ lead configurations (e.g. gull wings, BGA balls, passive components, etc.) on each test vehicle that can cause variation in defect results, and 2) there was not a large enough sample size for several of the component surface finishes (e.g. one component per test vehicle for palladium/silver SMT components) to provide an adequate comparison given the component package/lead variations.

Table 5.6: *SMT Defects by Component Finish*

Component Finish	Number of SMT Components	Defect Rate (Lead-free solder)	Defect Rate (Lead solder)
Tin/copper	144	0%	0%
Tin/bismuth	432	0.3%	0%
Tin	59,076	0.3%	0.8%
Gold	108	1.4%	0%
Tin/lead	468	2.1%	0%
Nickel/palladium/gold	612	3.1%	1.0%
Matte tin	324	5.1%	8.3%
Nickel/gold	240	9.1%	18.7%
SAC	168	13.5%	4.2%
Palladium/silver	36	16.7%	0%

There were five different THT component finishes used for the lead-free and tin/lead printed circuit boards. Table 5.7 illustrates the solder joint defect rate for each of the component finishes.

Table 5.7: *THT Defects by Component Finish*

Component Finish	Number of THT Components	Defect Rate (Lead-free solder)	Defect Rate (Lead solder)
Tin	576	15.1%	1.8%
Other lead-free	198	15.5%	2.3%
Tin/copper	54	17.4%	5.6%
Nickel/palladium/gold	36	20.8%	0%
Tin/nickel	90	46.7%	15.0%

5.5.5 Visual Inspection Observations

Several observations were noted by the inspectors during the visual inspection process. In general, the wetting for the lead-free solder joints was as good or better than the wetting of the tin/lead solder

joints. The lead-free solder flowed further up the lead than the tin/lead solder. For the component with gull wings, the heel fillet filled more than the toe fillet when using the lead-free solder paste. The lead-free combination with the best solder joints was considered to be printed circuit boards with the ENIG surface finish, laminate "Z", and solder paste "B".

A ten percent standard reduction was used for the apertures on the top stencil. The apertures for the bottom stencil included a 1 to 1 ratio with some exceptions (as noted earlier). In general, the components on the bottom had better overall solder joints, including much better wetting performance and fewer defects.

5.6 Reliability Testing

To better understand the reliability of the lead-free and tin/lead solder joints, thermal cycling and HALT was conducted on the Phase III printed circuit boards. The thermal cycling was performed at Raytheon's environmental testing facilities in Massachusetts. A Thermotron F125 chamber was used for the thermal cycling. Thermocouples were used to monitor the air temperature throughout the chamber. The thermal profile used for temperature cycling was selected to meet the requirements of IPC-9701, test condition TC1. These conditions were selected to facilitate direct comparison of our results with those of other investigators. The thermal cycling parameters are outlined below:

- Minimum temperature of 0° C, and maximum temperature of 100° C.
- Ramp rates (up and down): 10°C/min.
- Dwell times at maximum and minimum temperatures: 10 minutes.
- Number of thermal cycles selected: 2,000 cycles.

The highly accelerated lifetime testing (HALT) was conducted at Teradyne's facility in Massachusetts. A Qualmark HALT chamber was used for the HALT testing. The HALT parameters included temperature cycling between -60^{o} C and 160^{o} C, and vibration between static and 80 Grms. The root mean square acceleration (Grms) is used to express the overall energy of a particular random vibration event. A single 206 minute test cycle was conducted for each printed circuit board. Therefore, the printed circuit boards were not cycled to failure.

In addition, dynamic testing was done for seventeen daisy-chained links. Numerous components were included on each daisy chain. Figure 5.8 shows a Phase III printed circuit board in the HALT chamber with the daisy chain connection.

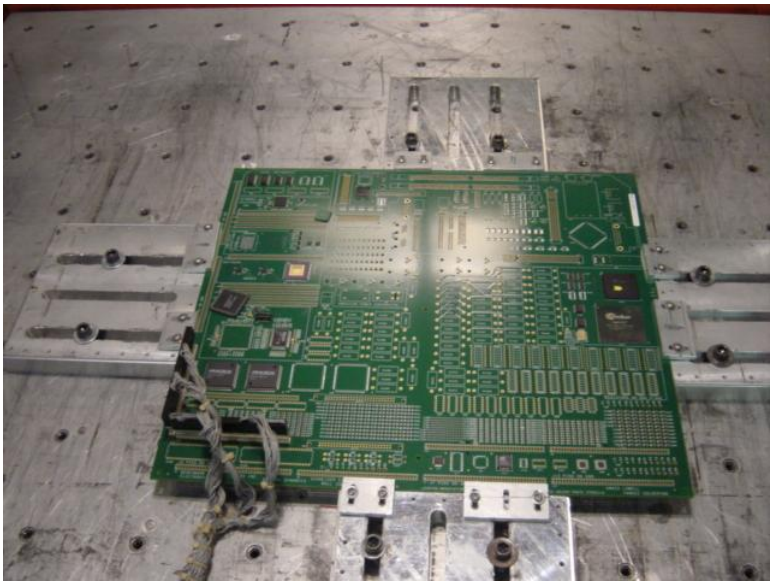

Figure 5.6. **Printed circuit board in HALT chamber.**

During the HALT testing, components U1 (plastic leaded chip carrier) and U78 (ball grid array) were considered to be the only component failures due to solder joint failures. Other component failures were due to lead fractures caused by the high mechanical stress. The HALT testing did not reveal any major differences between the reliability of the lead-free and tin/lead printed circuit boards. Visual inspection was conducted on the HALT printed circuit boards to further assess the validity of these preliminary conclusions.

5.7 Pull Testing

The test methodology consisted of using an Instron pull test machine to pull the leads of a component and record the maximum pull force. The following four components were included in the pull test:

- Two SOIC components with a tin finish
- Two SOIC components with a tin/bismuth finish

Four (4) leads were pulled on each of the SOIC components. The process of pulling the leads was as follows:

- The test vehicle was loaded at a 45 degree angle to the Instron machine and affixed with six screws to a specially designed hold down fixture. A 45 degree angle was chosen to measure both vertical and shear stresses.
- The leads adjacent to the ones pulled were removed (clipped) to facilitate pulling of target leads.

- The leads that were pulled were tied with a wire loop through the component leads. Fishing line (24-pound test) was used for pulling the SOICs.
- A new loop was made for each component pulled.
- The pull rate was 0.1 inch per minute, recording the peak pull force.
- The fractures were inspected and failure mode for each pull was noted.

The pull testing provided information for comparing the levels of solder joint strength between lead-free and tin/lead printed circuit boards, as well as comparing the solder joint strength before and after thermal cycling. Four spare test vehicles were pulled before thermal cycling, and eighteen test vehicles were pulled after thermal cycling.

5.8 Conclusions

Based on the visual inspection results, the solder joint integrity for surface mount technology components on the lead-free printed circuit boards was comparable to the tin/lead printed circuit boards for the selected solder paste suppliers, laminate suppliers, and board surface finishes. Therefore, attaining acceptable solder joint integrity with lead-free assembly is possible using existing equipment and with careful selection of materials. However, the rate of solder joint defects for THT components was higher for lead-free printed circuit boards than for tin/lead printed circuit boards. The Consortium members determined that further process optimization for THT components was needed.

The results from the post-HALT visual inspection indicate that: 1) the failure of two components (84 pin PLCC, BGA) was a result of solder joint failures, 2) other component failures were a result of lead fractures caused by high mechanical stress (e.g., through hole relay), and 3) no significant differences between lead-free and tin/lead boards were identified. In addition, after conducting the thermal cycling and the pull testing, it was determined that the strength of lead-free solder joints is comparable to lead solder joints for production-like boards. Finally, Consortium members decided to use Isola HR370 laminate material as a baseline lead-free laminate material for subsequent phases of research. [17]

6.0 PHASE IV RESEARCH EFFORTS

6.1 Overview

Phase IV research efforts were conducted from 2008 to 2011. The three major research areas for Phase IV included the assembly of test vehicles, rework with lead-free materials, and the reliability of lead-free electronics. This summary draws heavily from previous Phase IV reports, including "Evaluation of Lead-free Solders, Halogen-free Laminates, and Nanomaterial Surface Finishes for Assembly of Printed Circuit Boards", by Morose et al that was published in the Journal of Surface Mount Technology in 2009. [21]

6.1.1 Assembly of Test Vehicles

The first research area included an evaluation of the assembly of test vehicles using various lead-free, halogen-free and nano-materials. The lead-free materials evaluated during the assembly included the component finish, the board surface finish, the through-hole component solder, and the surface mount component solder paste. In addition, a halogen-free laminate material and a nano-material based surface finish were also included. The results of the lead-free assemblies were compared against baseline data obtained by assembling test vehicles with tin/lead materials. This research included the assembly of surface mount technology (SMT) and through-hole technology (THT) components. It was essential that quality lead-free solder joints were created during the initial assembly before subsequent research in rework and reliability areas could be undertaken.

6.1.2 Rework with Lead-free Materials

The second area of research was a comparison of rework capabilities for the various lead-free solders and surface finishes for through-hole components. During the assembly of printed circuit boards, the boards must often be reworked due to failures or defects encountered during the assembly process. This rework entails the removal and replacement of components onto the printed circuit board. Also, rework of printed circuit boards can occur anytime during the life of the electronic products. For example, if there were component failures during the use of the product, the printed circuit board may have to be sent back to the manufacturer for rework. Therefore, manufacturers want to be sure that their products can meet the rework requirements without failures due to using lead-free materials.

Phase IV research included the evaluation of three different rework processes using lead-free materials. It also included the evaluation of a rework nozzle that was specifically designed and fabricated to address the rework challenges encountered when using lead-free materials. This rework nozzle was an early prototype and was not commercially available at the time of the research effort. There has not yet been any experiments or research conducted for this new rework nozzle design.

6.1.3 Reliability of Lead-free Electronics

The third research area was an evaluation of the long-term reliability of test vehicles that were assembled using lead-free materials. This is of concern to companies that manufacture products that require high reliability and a product life of five or more years. These manufacturers want to ensure that

their products can meet long-term product life requirements without failures due to using lead-free materials.

The long-term reliability testing was based on accelerated testing techniques to assess the product life of these electronic assemblies. The primary testing techniques used for the reliability testing were thermal cycling and internal stress testing. The results of this research included a comparison against baseline data for test vehicles assembled using tin/lead solder. The research results should help to further advance the electronic products industry towards the implementation of lead-free electronics for all applications, including those demanding high reliability and long product life.

To provide research of value to the electronic products industry, a key step is to use industry-accepted standards and guidelines for research conducted in the areas of assembly, rework, and reliability. The Association Connecting Electronics Industries (IPC) is a trade organization dedicated to furthering the competitive success of its members in the electronic products industry. IPC has developed industry standards for various electronic assembly activities such as fabrication, acceptance, assembly, inspection, solderability, and testing of printed circuit boards. Throughout the documentation for this research, IPC standards were referenced and adhered to whenever possible. This is necessary to ensure that companies in the electronic products industry can accept the validity of these research results.

The equipment and materials required for the research in all three areas were obtained by donations by member companies from the New England Lead-free Electronics Consortium, as well as funding provided by the U.S. EPA. The following individuals and organizations provided contributions and support during this phase of research efforts:

- Greg Morose, Toxics Use Reduction Institute
- Sammy Shina, University of Massachusetts Lowell
- John Goulet, JoAnn Newell, Robert Farrell, Paul Bodmer, Bruce Tostevin, Allen Ouellette, and Scott Mazur, Benchmark Electronics
- Mike Havener, Benchmark Electronics
- David Pinsky, Amit Sarkhel, and Karen Ebner, Raytheon
- Rob Tyrell, Stentech
- Don Lockard, Yankee Soldering
- Eric Renn and Deb Fragoza, EMC
- Andy Lesko and Bernhard Wessling, Ormecon
- Don Longworth, Tom Buck, and Wendi Boger, Dynamic Details Inc.
- Linda Darveau, U.S. EPA Region 1
- Helena Pasquito and Dick Anderson, Cobham (M/A-COM)
- George Wilkish, Prime Consulting
- Roger Benson, Carsem
- Scott Miller, Wendy Milam, and Lauren Primmer, Freedom CAD
- Crystal Wang, International Rectifier
- Don Abbot, Texas Instruments
- Ken Degan, Teradyne
- Steven Sekanina, Isola

- Mike Jansen, Mike Miller and Louis Feinstein Textron Systems
- Charlie Bickford, Wall Industries
- Paul Reid and Bill Birch, PWB Interconnect Solutions
- Tim O'Neill and Karl Seelig, Aim Solder
- Lou Wroblewski, Premier Tool Works

6.2 Experimental Design

The research included numerous types of lead-free materials to be used for assembly, rework, and reliability testing efforts. The Consortium members selected materials and components that had appropriate temperature ratings for lead-free electronics assembly. There were 30 different types of surface mount components and 10 different types of through-hole components included in this research.

The research included four different printed circuit board surface finishes. The purpose of the surface finish is to provide solderability protection, a contact surface, and a solder joint interface. [18] The first finish included was electroless nickel immersion gold (ENIG). This surface finish involved using both electroless and immersion technologies to deposit the metallic surface finish.

The second finish included was hot air solder leveling (HASL) technology to apply the surface finish to the printed circuit board. HASL is a method that entails dipping a bare printed circuit board that into a solder bath. The excess solder is then removed from the printed circuit board by an air stream. [19] For this research, the HASL surface finish used the tin/copper lead-free alloy was with 99.4% tin and approximately 0.6% copper.

The third surface finish used an organic protection system for the copper pads on the printed circuit board. This surface finish is referred to as organic solderability preservatives (OSP).

The fourth surface finish included for this research was a surface finish using nano materials. The nano surface finish consists of nano silver particles (approximately 4 nm) dispersed in a polymer (polyaniline). The thickness of the nano surface finish applied to the test vehicles is approximately 50 nm. This finish is referred to as an organic metal finish. Ninety percent of the surface finish by volume is organic metal (polyaniline), and nano silver particles comprise the remaining 10%. [20]

Solder paste is comprised of the solder alloy and a flux that is necessary to clean the surfaces that are to be soldered. This research included the following four different solder pastes for assembly of the surface mount components.

- Tin/silver/copper alloy (SAC305, 96.5% tin, 3% silver, and 0.5% copper) with no clean chemistry flux (from two different suppliers)
- Tin/silver/copper alloy (SAC305) with organic acid chemistry flux
- Tin/lead alloy with no clean chemistry flux for baseline purposes

Three different solder alloys were used in this research for the assembly of the through-hole components. The solders used were as follows:

- Tin/silver/copper alloy (SAC305)
- Tin/copper alloy (99.4% tin, 0.6% copper)
- Tin/lead alloy (63% tin and 37% lead, lead-tin eutectic alloy) for baseline purposes

For this research, the three factors under investigation in the Design of Experiments were surface mount component solder paste, through-hole component solder, and surface finish. The Design of Experiments (including solder paste, solder, and surface finish) that was used for the 24 lead-free test vehicles is provided in Table 6.1. [21]

Table 6.1: ***Lead-free Test Vehicles – Design of Experiments***

Test Vehicle	SMT Solder Paste	Through Hole Solder	Surface Finish
1	SAC 305 NC-1	SAC305	ENIG
2	SAC 305 NC-1	SAC305	ENIG
3	SAC 305 NC-1	SAC305	LF HASL
4	SAC 305 NC-1	SAC305	LF HASL
5	SAC 305 NC-1	SAC305	OSP
6	SAC 305 NC-1	SAC305	OSP
7	SAC 305 NC-1	SAC305	Nanofinish
8	SAC 305 NC-1	SAC305	Nanofinish
9	SAC 305 (OA)	Tin/copper (295 ^{o}C)	ENIG
10	SAC 305 (OA)	Tin/copper (295 ^{o}C)	ENIG
11	SAC 305 (OA)	Tin/copper (295 ^{o}C)	LF HASL
12	SAC 305 (OA)	Tin/copper (295 ^{o}C)	LF HASL
13	SAC 305 (OA)	Tin/copper (295 ^{o}C)	OSP
14	SAC 305 (OA)	Tin/copper (295 ^{o}C)	OSP
15	SAC 305 (OA)	Tin/copper (295 ^{o}C)	Nanofinish
16	SAC 305 (OA)	Tin/copper (295 ^{o}C)	Nanofinish
17	SAC 305 NC-2	Tin/copper (310 ^{o}C)	ENIG
18	SAC 305 NC-2	Tin/copper (310 ^{o}C)	ENIG
19	SAC 305 NC-2	Tin/copper (310 ^{o}C)	LF HASL
20	SAC 305 NC-2	Tin/copper (310 ^{o}C)	LF HASL
21	SAC 305 NC-2	Tin/copper (310 ^{o}C)	OSP
22	SAC 305 NC-2	Tin/copper (310 ^{o}C)	OSP
23	SAC 305 NC-2	Tin/copper (310 ^{o}C)	Nanofinish
24	SAC 305 NC-2	Tin/copper (310 ^{o}C)	Nanofinish

The Design of Experiments that was used for the eight tin/lead test vehicles is provided in Table 6.2. These tin/lead test vehicles provided a baseline for comparison with the lead-free test vehicles.

Table 6.2: ***Tin/Lead Boards - Design of Experiments***

Board	SMT Solder Paste	Through Hole Solder	Surface Finish
25	Tin/lead NC	Tin/Lead	ENIG
26	Tin/lead NC	Tin/Lead	ENIG
27	Tin/lead NC	Tin/Lead	LF HASL
28	Tin/lead NC	Tin/Lead	LF HASL
29	Tin/lead NC	Tin/Lead	OSP
30	Tin/lead NC	Tin/Lead	OSP
31	Tin/lead NC	Tin/Lead	Nanofinish
32	Tin/lead NC	Tin/Lead	Nanofinish

6.3 Methodology

This section outlines the methodology used for the assembly of test vehicles, rework with lead-free materials, and the reliability of lead-free electronics.

6.3.1 Assembly of Test Vehicles Methodology

Figure 6.1 shows the assembled test vehicle that was used for the basis of this research phase. The test vehicle was 0.110 inches thick, 8 inches wide, 10 inches long, had twenty layers of copper, and contained both surface mount and through-hole components. The Consortium members chose a thick board with a high thermal load because it is more challenging to assemble and rework. Also, the research results can be extrapolated to thin boards with low thermal loads.

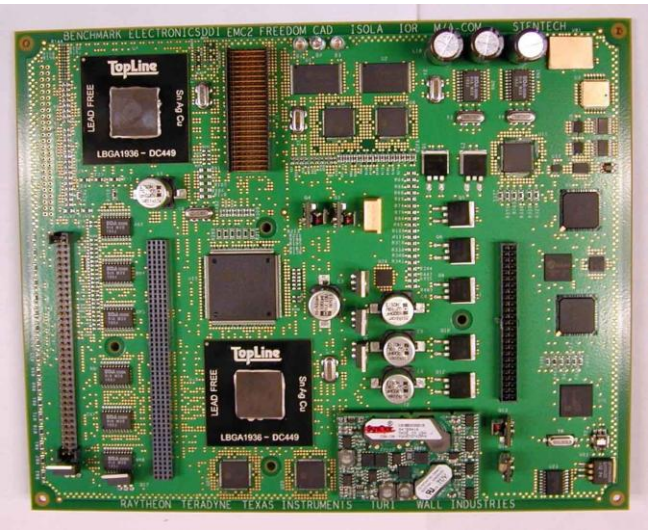

Figure 6.1. **Assembled phase IV test vehicle.**

There were 886 surface mount components and 21 through-hole components assembled on each test vehicle. The test vehicles were manufactured by Dynamic Details Inc. at their board fabrication plant in Sterling, Virginia. The assembly and inspection of the components to the lead-free and tin/lead test vehicles was handled by Benchmark Electronics.

The temperature profile of the test vehicle and surface mount components during passage through the reflow oven is a critical determinant of solder joint quality. It was very challenging to obtain a desirable thermal profile for the test vehicle used in Phase IV because the test vehicle was thick (0.110") and contained many different types of components with greatly varying thermal masses and orientation.

Lead-free solder paste using the SAC 305 alloy solder melts at 217 to 220 ^{o}C, and the time that is spent above this temperature while in the reflow oven is called time above liquidus (TAL). The three lead-free solder pastes used in this research contained the lead-free SAC alloy. The target peak reflow temperature for test vehicles assembled with lead-free solder was in the range of 240 to 248 ^{o}C, and the target time above liquidus is in the range of 60 to 90 seconds. The target thermal profile was a ramp-to-peak method. The actual top side reflow temperature profile measured by five thermocouples (TC# 2 through TC #6) for the lead-free test vehicles can be seen in Figure 6.2.

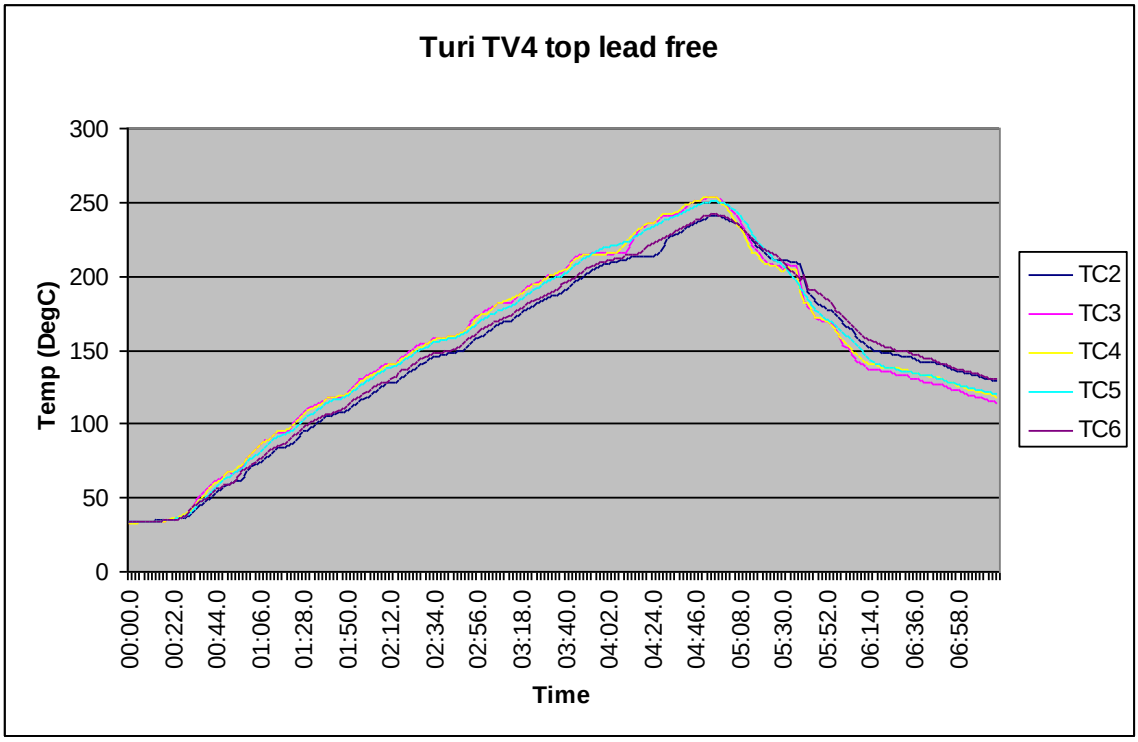

Figure 6.2. **Top side reflow profile for lead-free test vehicles.**

The second reflow temperature profile was for the tin/lead solder paste that melts at 183 ^{o}C. The target peak temperature in the reflow oven for test vehicles assembled with tin/lead solder was in the range of 210 to 218 ^{o}C, and the target time for the test vehicles to be above the liquidus temperature was in the range of 60 to 90 seconds.

The third reflow temperature profile generated was for the top side of the test vehicles assembled with tin/lead solder paste. The top side of these test vehicles contained ball grid array (BGA) components that contained lead-free solder balls. Therefore, a hybrid reflow temperature profile was needed to melt the tin/lead solder pastes as well as the lead-free solder on the BGA components. The target peak temperature for the hybrid profile was in the range of 222 to 230 ^{o}C, and the target time above liquidus is in the range of 60 to 90 seconds. [22]

The three major steps for the assembly of the through-hole components were flux application, preheating, and soldering. The flux needs to be applied to each through hole on the test vehicle prior to soldering to help prevent the oxidation of the metal that may occur at the elevated soldering temperatures. The flux was applied automatically to the bottom side of the test vehicle.

Preheating the test vehicle was necessary to minimize the thermal stress that occurs when the test vehicle is exposed to the high soldering temperatures. The intent was to gradually raise the temperature of the test vehicle closer to the soldering temperature to minimize thermal stress. However, the preheat temperature cannot be too high or it may burn off the flux before the soldering occurs. For this research, the target preheat temperature was between 110 and 115 ^{o}C.

The IPC-A-610 Revision D standard was used as the guideline for conducting the visual inspection for this research. This standard is a collection of visual quality acceptability requirements that is used for electronic assemblies. The standard provides different requirements depending on the classification of the electronic products assembly. The visual inspection for this research was conducted to meet the requirements of Class 3, High Performance Electronic Products. This classification was chosen because it covers electronic assemblies that must meet high reliability applications. [23] For this research, only soldering-related defects were considered.

6.3.2 Rework With Lead-free Materials Methodology

The Consortium members established the following criteria for the rework success of through-hole components:

- Meet IPC Class III visual inspection criteria
- No laminate material degradation (e.g. delamination, pad lifting)
- Achieve minimal copper dissolution: primary target is to meet 0.001" minimum copper thickness at the knee (Class 3), secondary target is 0.0008" minimum copper thickness (Class 2)

The rework effort was conducted on rework coupons, and not on the actual test vehicles. The panel design included both test vehicles and rework coupons to ensure that the rework research was done on the same laminate material and board stackup as the actual test vehicles.

The through-hole component selected for the through hole rework process was the Samtec 200 pin connector. This component was selected because it would be a challenge to successfully rework this component given the thickness of the rework coupon (0.110 inches). Figure 6.3 shows the Samtec 200 pin through hole connector mounted on the upper left hand corner at component location J5 of the rework coupon.

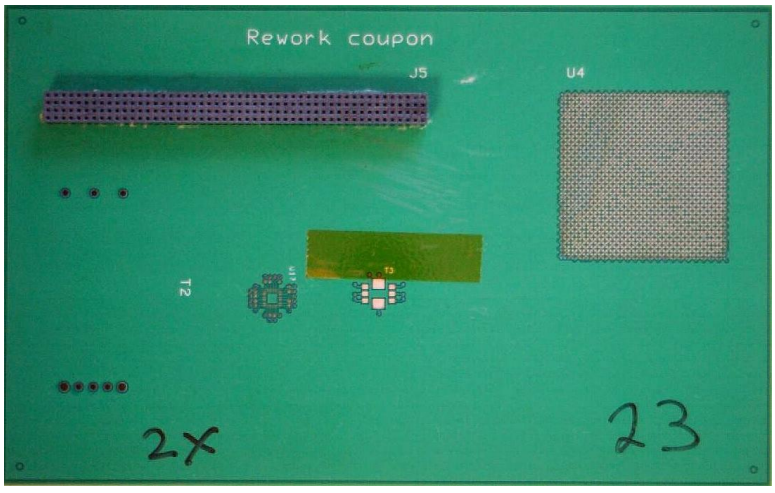

Figure 6.3. **Rework coupon with through-hole connector.**

The through-hole component rework process included four surface finishes: OSP, ENIG, lead-free HASL (using the tin/copper alloy), and nano. Nine rework coupons with OSP surface finish were sent to Ormecon to apply the nano surface finish. Applying the nanosurface to bare copper is the preferred method by Ormecon, but the only rework coupons available for this research already had the OSP surface finish applied. Consequently, the OSP finish had to be stripped off by Ormecon before applying the nano surface finish. It is difficult to strip the coupon of its previous surface finish while maintaining an optimal, homogenous copper surface. This may have affected the visual appearance of the nanofinish and the solderability of the coupons. [24]

Two different lead-free solder alloys were used for this rework experiment: SAC 305 solder and tin/copper solder. Because of time and resource constraints, the tin/lead solder was not included as a baseline measurement for these efforts.

There were 24 rework coupons included in the through-hole component rework effort. This provided a balanced Design of Experiments for the rework efforts. The rework process took place at Benchmark Electronics in New Hampshire. The rework coupons had to undergo two passes through the reflow oven to simulate the thermal stresses that would have been encountered during an actual surface mount assembly process.

The primary machine that was used for the rework efforts was the Premier Rework RW116 machine. There were two types of nozzles used on the Premier Rework machine for the rework efforts. The first was a standard nozzle, shown in Figure 6.4.

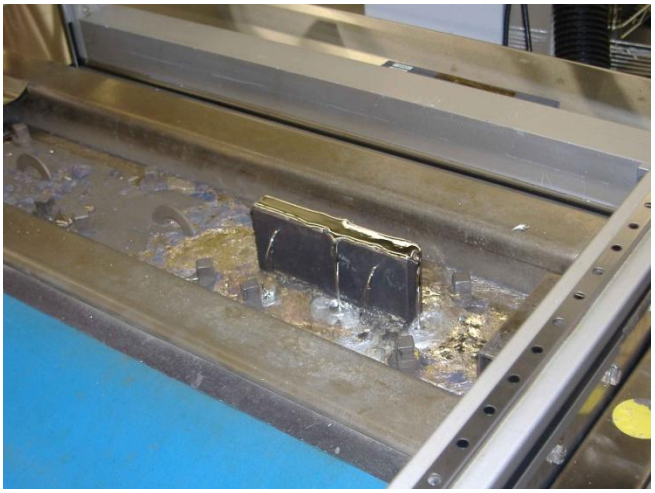

Figure 6.4. **Standard nozzle during rework operations.**

The second type of nozzle used for the through-hole rework was a hybrid nozzle. The hybrid nozzle was a special proprietary design to address the challenges of copper dissolution during the rework process with lead-free solders. The intent of the design was to minimize solder flow at the surface of the test vehicle but also to maintain adequate heat transfer to the solder to avoid a significant drop in solder temperatures during rework operations. Figure 6.5 shows the hybrid nozzle with solder flow during actual rework operations.

Figure 6.5. **Hybrid nozzle during rework operations.**

Three different rework processes were used for reworking the through-hole components. For each of these processes, a board preheat temperature of 130 ^{o}C was used for the rework machine, and Alpha EF2202 no-clean flux was used at the component site. These three processes were:

Process 1: The Premier Rework RW116 machine was used for initial component installation, component removal and second component installation. This process used the standard nozzle design.

Process 2: The Premier Rework RW116 machine was used for initial component installation, component removal and second component installation. This process used the hybrid nozzle design.

Process 3: The Premier Rework RW116 was used for the initial and second component installation. This process used the standard nozzle design for component installation. The Air-Vac DRS25 was used for component removal. Previous studies have found that forced convection for component removal together with solder fountain for component installation during rework can have an impact on decreasing copper dissolution rates. [25]

The objective was to have a solder pot temperature of 270 ^{o}C for the SAC 305 solder. The tin/copper solder has a higher melting temperature than SAC305, so it is best to use this solder at a higher temperature. Therefore, the solder pot temperature was raised to 287 ^{o}C for the tin/copper solder. For Process 3, the component removal was accomplished by using the Air-Vac DRS25XLT machine. The rework coupon was preheated prior to the start of reflow. Once the reflow was complete, the heat nozzle was taken off the component so that the connector could be removed from the rework coupon.

After the connector was removed from the rework coupon, heat was continuously applied to the rework coupon, and finally the vacuum nozzle was used to remove the solder from the connector holes. The key measurements made during the through-hole rework process were contact time and copper dissolution rate. The contact time, when the solder in the nozzle is in contact with the bottom surface of the rework coupon, was measured for each step in the rework process. For Processes 1 and 2, this included contact

time during initial component installation, component removal, and second component installation. For Process 3, this included contact time during initial component installation and second component installation. Microsectional analysis was used to evaluate the level of copper dissolution. Microsections of the connector and rework coupon were conducted to obtain copper dissolution measurements.

6.3.3 Reliability Testing Methodology

Thermal Cycling

Thermal cycle testing to a 63% failure rate was conducted to characterize the failure distribution. This test included continuous monitoring of the daisy chains on the test vehicle by a data logger. Failure was defined as a maximum of 20% nominal resistance increase for a daisy chain circuit within a maximum of five consecutive reading scans.

The test vehicles used for the thermal cycling were the same that were used for the assembly section of this report. Each of the test vehicles had 14 daisy chain electrical connections for monitoring solder joint integrity during the actual testing. The thermal cycling included 16 test vehicles to cover each of the factor combinations in the Design of Experiments. In addition, two test vehicles using the halogen-free laminate were also included, resulting in a total of eighteen test vehicles for the thermal cycling test.

The thermal cycling done for this research included one exception to the IPC-9701 standard: The dwell time at the temperature extremes was 15 minutes instead of 10 minutes for the thermal cycling. The IPC standard was developed to primarily address tin/lead solder materials. SAC solders have a lower creep rate than tin/lead solders at thermal cycle temperatures. This limits the amount of SAC solder damage during a short dwell time. Increasing the dwell time during thermal cycling for SAC solder has been reported to cause a decreasing characteristic lifetime for typical thermal cycling conditions. [26] The intent of changing to a fifteen minute dwell time was to provide additional time to allow creep for the lead-free solders to reach completion.

The monitoring during thermal cycling consisted of resistance testing for the 14 daisy chain circuits on each of the 18 test vehicles. The 14 daisy chains on the test vehicle were all routed to two pins in the area of the fifty pin through hole connector (RefDes J2) location. The monitoring for the thermal cycling was conducted by using a data logger. The data logger required a total of 252 channels to monitor all of these daisy chains.

The Agilent data logger used during the thermal cycling was capable of scanning as many as 100 channels per second. Therefore, all 252 channels were able to be scanned in less than five seconds. This scanning rate satisfies the IPC 9701 requirement that the maximum scan interval for all daisy chains be one minute or less.

Four of the fourteen daisy chains on the test vehicles were connected to discrete components (i.e. 0402, 0603, and 0805 resistors). Each of these daisy chains contained approximately 50 to 100 discrete components connected in series. Therefore, monitoring of these daisy chains only detected the first failure for each of the daisy chains on each of the test vehicles. Consequently, we were not able to determine when 63% failure occurs for discrete components.

The other ten daisy chains on the test vehicle were connected to only one component per daisy chain. The daisy chain was connected to each solder joint of the component. For example, a TSOP component with 48 pins has all 48 solder joints connected in series. If one solder joint of the component failed, then the data logger detected a failure for that daisy chain.

Monitoring of the ten daisy chains with single components provided first failure information for the experiment, as well as when the 63% failure threshold occurred for each component type. For example, pin number 33 and 34 on the J2 connector formed a daisy chain connection for a microBGA (Reference Designator U26) provided by Benchmark Electronics. We were able to detect when the first failure occurred for this microBGA. This first failure could occur on any of the 18 test vehicles. We were also able to detect when at least 63% component failure occurred. For this testing plan, 63% failure occurred when the microBGA failed on 12 out of the 18 test vehicles.

A complete listing of the daisy chain connections can be seen in Table 6.1. The table includes the J2 pin numbers that the daisy chain is routed to, as well as a description of the components that were connected to each daisy chain. During the test vehicle design, a net list was created and used to specify all the daisy chain connections to be routed during the fabrication of the test vehicle.

Table 6.1: ***Daisy Chain Connections on the Test Vehicle***

J2 Connector Pin Numbers	Component RefDes	Component Type	Qty.
22, 21	R2 to R472	0402 Resistor, 0 ohm	100
18, 17	R21 to R499	0603 Resistor, 0 ohm	100
16, 15	R5 to R462	0805 Resistor, 0 ohm	49
14, 13	R15 to R493	0805 Resistor, 0 ohm	52
10, 9	U1	SMT, TSOP, 48 Pins	1
8, 7	U2	SMT, TSOP, 48 Pins	1
6, 5	U24	SMT, TSOP, 48 Pins	1
4, 3	U25	SMT, TSOP, 48 Pins	1
2, 1	U15	SMT, PQFP208	1
48, 47	U14	SMT, Plastic BGA, 256 balls, 1.0 mm pitch	1
45, 44	U18	SMT, Plastic BGA, 256 balls, 1.0 mm pitch	1
42, 41	U16	SMT, Chip array BGA, 100 balls, 1.0 mm pitch	1
40, 39	U17	SMT, Tape array uBGA, 64 balls, 0.5 mm pitch	1
34, 33	U26	SMT, Ceramic u-BGA, 0.5mm pitch	1

It was necessary to create cable assemblies to connect the daisy chain terminations at the J2 location on the test vehicle to the data logger D-Sub style connectors. Due to the concern of potential intermittent connector failures during thermal cycling due to vibration inherent within a thermal chamber, it was

deemed necessary to solder each of the wires to the test vehicle that connect the test vehicle daisy chains to the data logger.

A specification was developed for all the interconnections for this cable assembly. A high temperature rated wire was used for the cable assembly to ensure the wire could withstand the temperature extremes within the thermal cycling chamber. The wire used had high reliability Teflon insulation and was rated for use up to 200 ^{o}C. The cable assembly process was undertaken by technicians from Wall Industries during 2008. A Tektronix DMM914 True RMS meter was used to measure the resistance values for each cable connection.

The thermal cycling at two locations: the Cobham (M/A-COM) facility in Lowell, MA, and the Textron Systems facility in Wilmington, MA. The thermal cycling chambers at each of these three facilities have the capability to meet the target thermal cycling parameters outlined later in this section. Based upon availability of thermal chamber space, the test vehicles and the data logger were moved from one location to another as necessary until the thermal cycling testing was completed.

Prior to thermal cycling, all assembled test vehicles received accelerated thermal aging consisting of a bake-out period of 24 hours at 100 ^{o}C. The parameters used for the thermal cycling included a high temperature of 125 ^{o}C and a low temperature of -55 ^{o}C, resulting in a total temperature differential of 180 ^{o}C between the high and low temperature extremes. These maximum and minimum temperatures were based upon IPC-9701, test condition #4. Both the high and low temperature dwell times were fifteen minutes. The temperature ramp rate was approximately 5 ^{o}C per minute. Therefore, the overall cycle time was 102 minutes (36 minutes temperature ramp up + 15 minutes high temperature dwell + 36 minutes temperature ramp down + 15 minutes low temperature dwell). The thermal profile is illustrated in Figure 6.6.

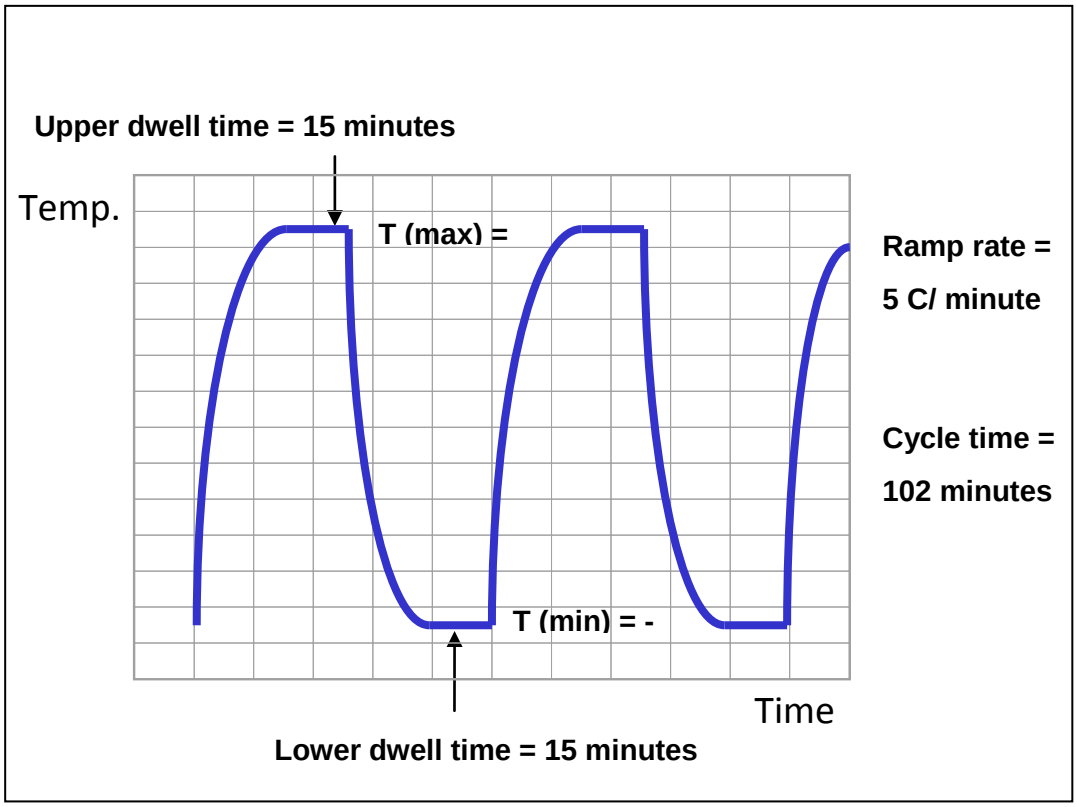

Figure 6.6. **Thermal cycling temperature profile.**

The thermal cycling efforts at the Textron Systems facility used a Thermotron Model F-32-CHV-705 thermal chamber. The chamber was rated for operating temperatures between -73 ^{o}C to plus 177 ^{o}C. The total cycle time was 102 minutes, resulting in approximately 98.8 cycles per week.

Four card racks were needed to hold the eighteen test vehicles in the chamber. These card racks were purchased with funding provided by the U.S. EPA. The test vehicles were mounted on two levels, with each level containing two card racks and nine test vehicles.

The thermal cycling conducted at the Cobham (M/A-COM) facility used a Tenney Environmental Model T20C-1.5 thermal chamber. In addition, a Watlow F4 controller and Watview software were used to control the thermal chamber.

6.4 Results

This section outlines the results achieved for the assembly of test vehicles, rework with lead-free materials, and the reliability of lead-free electronics.

6.4.1 Assembly Research Results: Through-Hole Components

For this research, Analysis of Variance (ANOVA) was utilized to understand the relationship between the lead-free materials used and the assembly results. The overall mean for defects per test vehicle for all combinations was 105 defects per test vehicle. The two best-performing through-hole component solders were tin/copper (2) and the SAC305 solders, with 79 and 96 defects per test vehicle, respectively. The two lesser-performing solders were tin/lead and tin/copper (1) solders, with 115 and 131 defects per test vehicle, respectively. The two best-performing surface finishes were lead-free HASL and ENIG surface finishes, with 51 and 84 defects per test vehicle, respectively. The two lesser-performing surface finishes were the OSP and nano surface finishes, with 142 and 143 defects per test vehicle, respectively. The results of the main effects are shown in Figure 6.7.

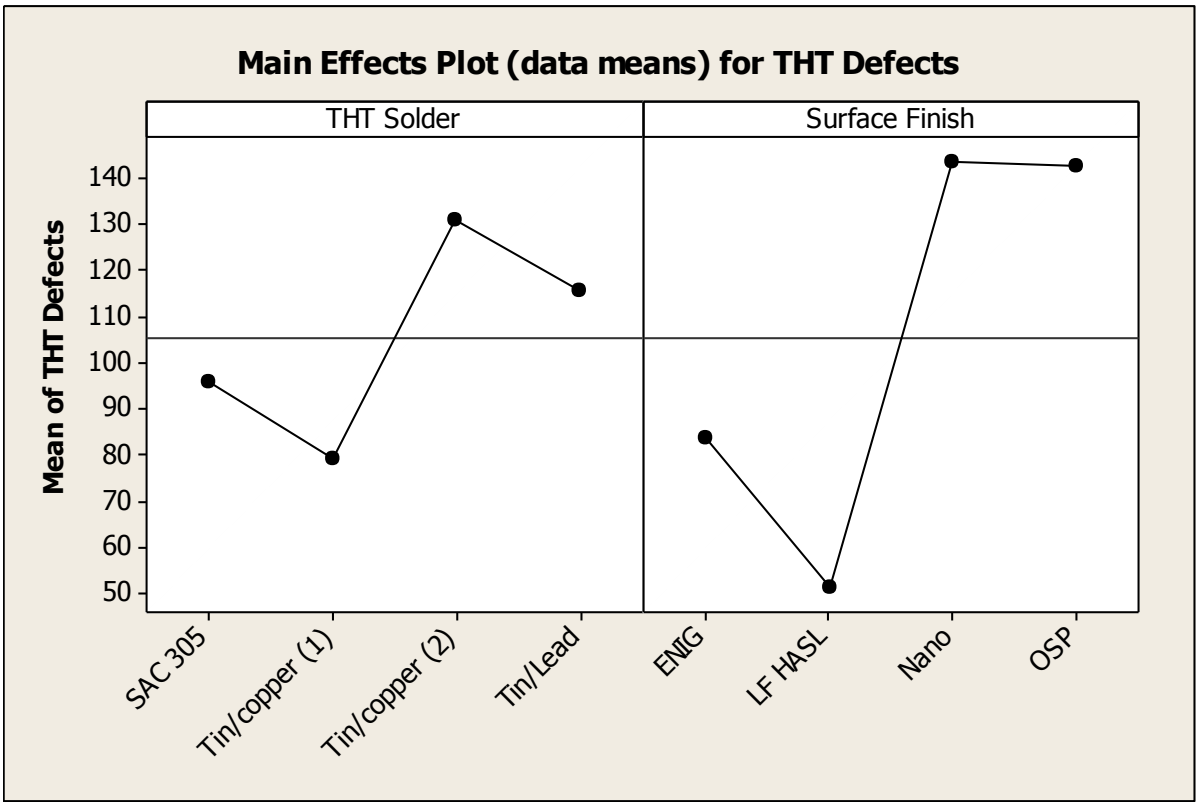

Figure 6.7. **Main effects plot for through-hole component defects.**

The interaction plot reveals that the ENIG surface finish varied widely across the different solder types. The ENIG surface finish had the lowest defect rate when using the SAC305 and tin/lead solders, but it had the highest defect rate when used with the tin/copper (1) and tin/copper (2) solders. The lead-free HASL had the lowest defect rate for the tin/copper (1) and tin/copper (2) solders, and had the second lowest defect rate for SAC 305 and tin/lead solders. This positive result was expected given that the lead-free HASL finish is comprised of the tin/copper solder alloy. The lead-free HASL surface finish is a good choice for a company that may use more than one solder type. The performance of the nano and OSP surface finishes were comparable for each of the four solders. Figure 6.8 illustrates the effect of the interactions for the various combinations.

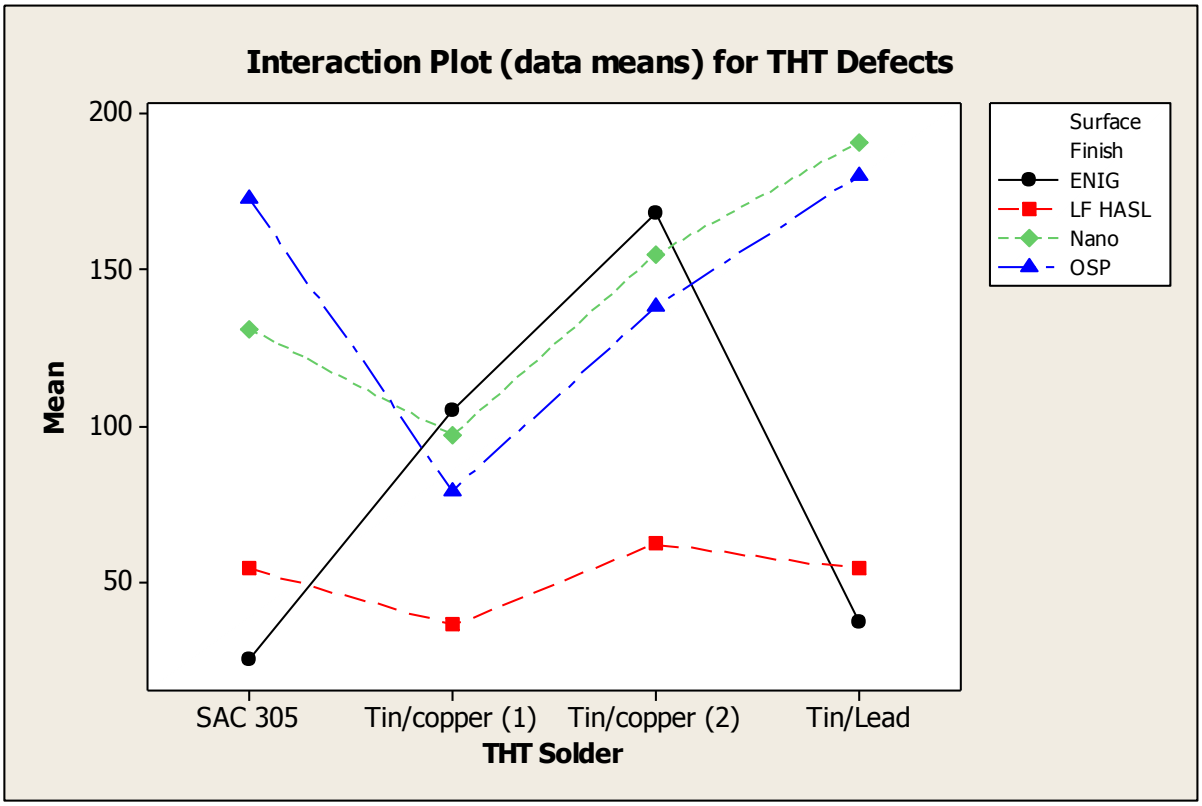

Figure 6.8. **Interactions plot for through-hole component defects.**

6.4.2 Assembly Research Results: Surface Mount Components

Upon review of the mean values and the main effects plot for this research, it was determined that the SAC 305 OA solder paste had a much higher mean defect rate (8.0 defects per test vehicle) than the overall average rate (4.25 defects) and the rates of the other three solder pastes. The other three solder pastes (SAC 305 NC-1, SAC 305 NC-2, and tin/lead NC) had defect rates between 2.75 and 3.25 defects per test vehicle and each had no-clean flux. For the surface finishes, it can be seen that the nano surface finish had the lowest mean defect rate (2.75 defects per test vehicle), while the other three surface finishes had defect rates between 4.0 and 5.5 defects per test vehicle. Figure 6.9 is the main effects plot for the surface mount components for all solder types.

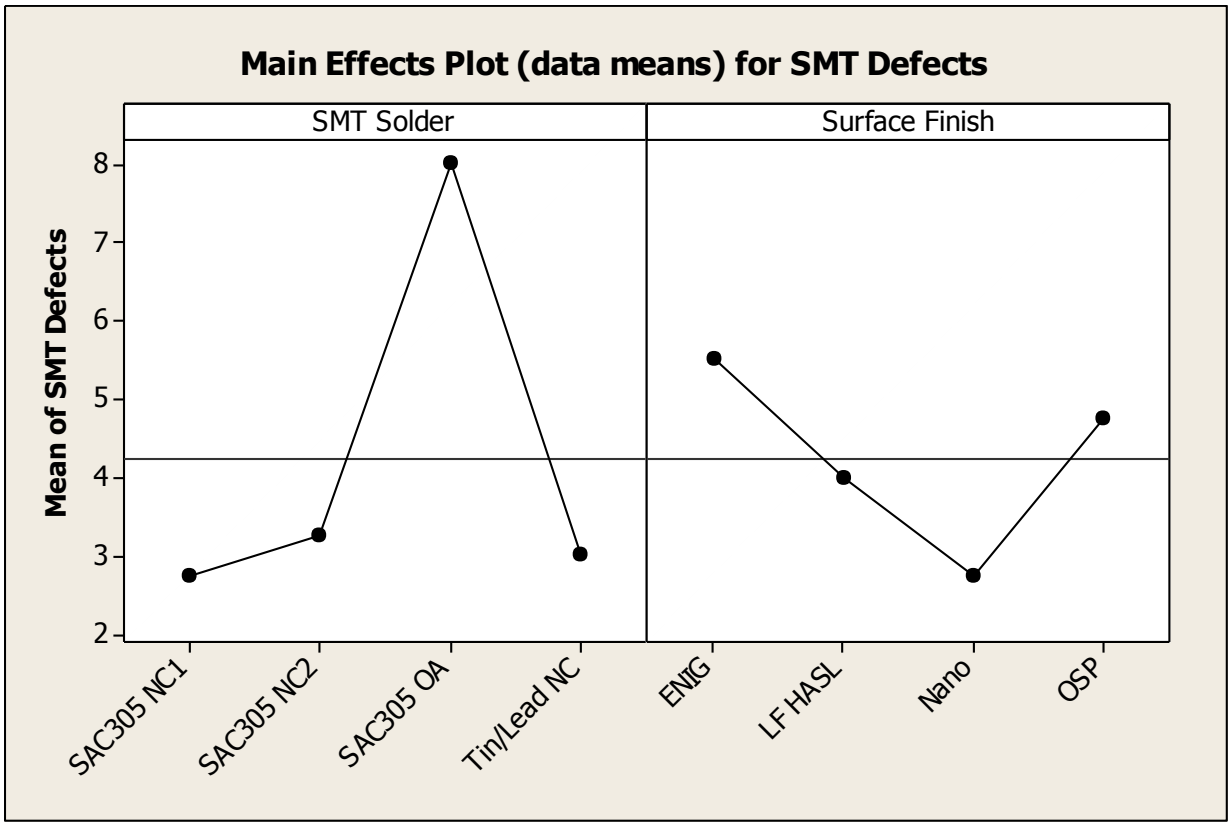

Figure 6.9. **Main effects plot for the surface mount components for all solder types.**

6.4.3 Rework with Lead-free Materials Results

Contact Time

Upon review of the means for the main effects and the main effects plot, it was found that the SAC 305 solder had a low mean contact time of 65 seconds as compared to 88 seconds for tin/copper solder. Process #1 also had a low mean contact time, 68 seconds, as compared to the mean contact time of 139 seconds for Process #2. The only difference between these two processes was the type of nozzle used. Process #1 used the standard nozzle and Process #2 used the hybrid nozzle. The contact time required for solder flow through to the topside of the rework coupon was much greater for the hybrid nozzle than for the standard nozzle. Process #3 had the lowest mean contact time, 32 seconds, because there was no contact time during the component removal process when using the Air-Vac machine.

The mean contact time for the ENIG (72 seconds), nano (70 seconds), and HASL (77 seconds) surface finishes were all between 70 to 77 seconds. The contact time for the OSP surface finish was the highest of the four surface finishes with a mean time of 89 seconds. Figure 6.10 is the main effects plot for contact time.

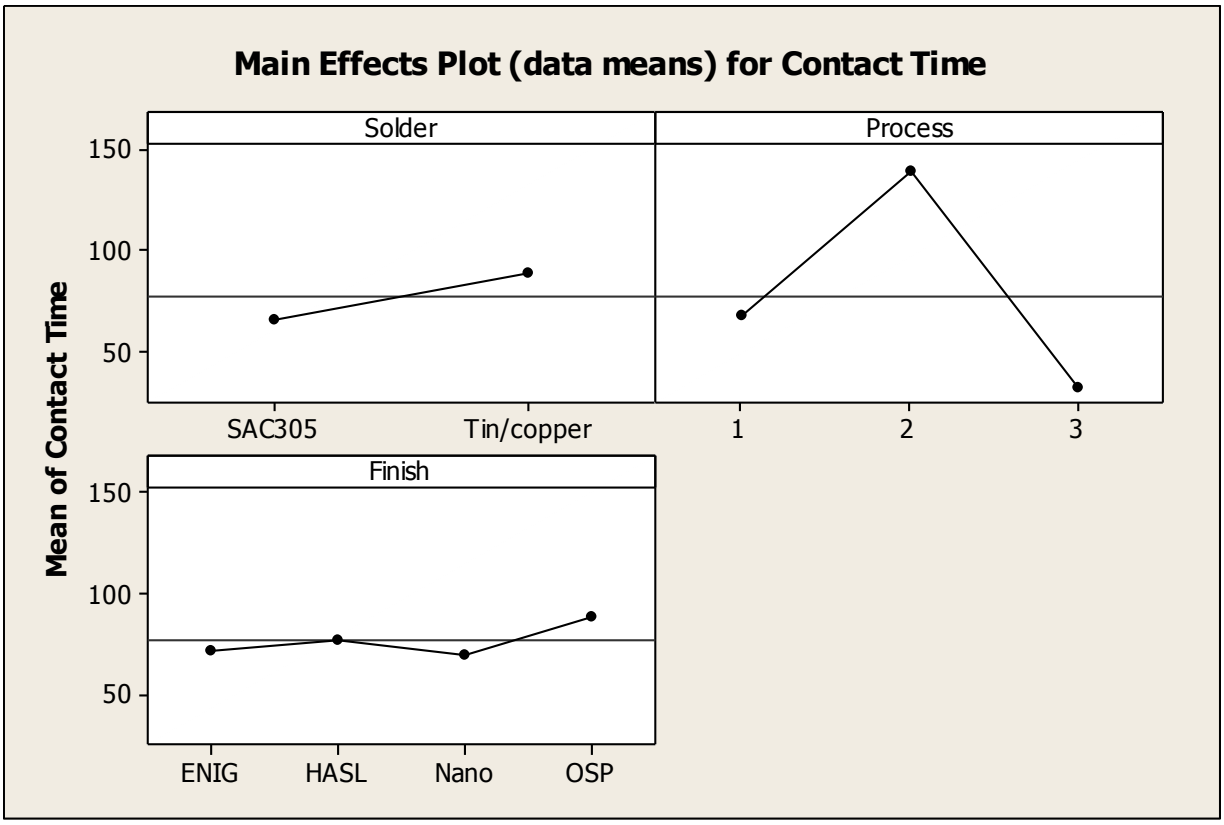

Figure 6.10. **Main effects plot for contact time.**

Upon review of the interaction plot, it appears that the main effect of the process was predominant over any of the possible interactions. For example, Process #2 had the highest contact time for all four surface finishes (ENIG, HASL, Nano, and OSP), Process #1 had the second highest contact time for all four surface finishes, and Process #3 had the lowest contact time for all four surface finishes. In addition, Process #2 had the highest contact time for both solders (tin/copper and SAC305), Process #1 had the second highest contact time for both solders, and Process #3 had the lowest contact time for both solders. Figure 6.11 shows the interaction plot for contact time.

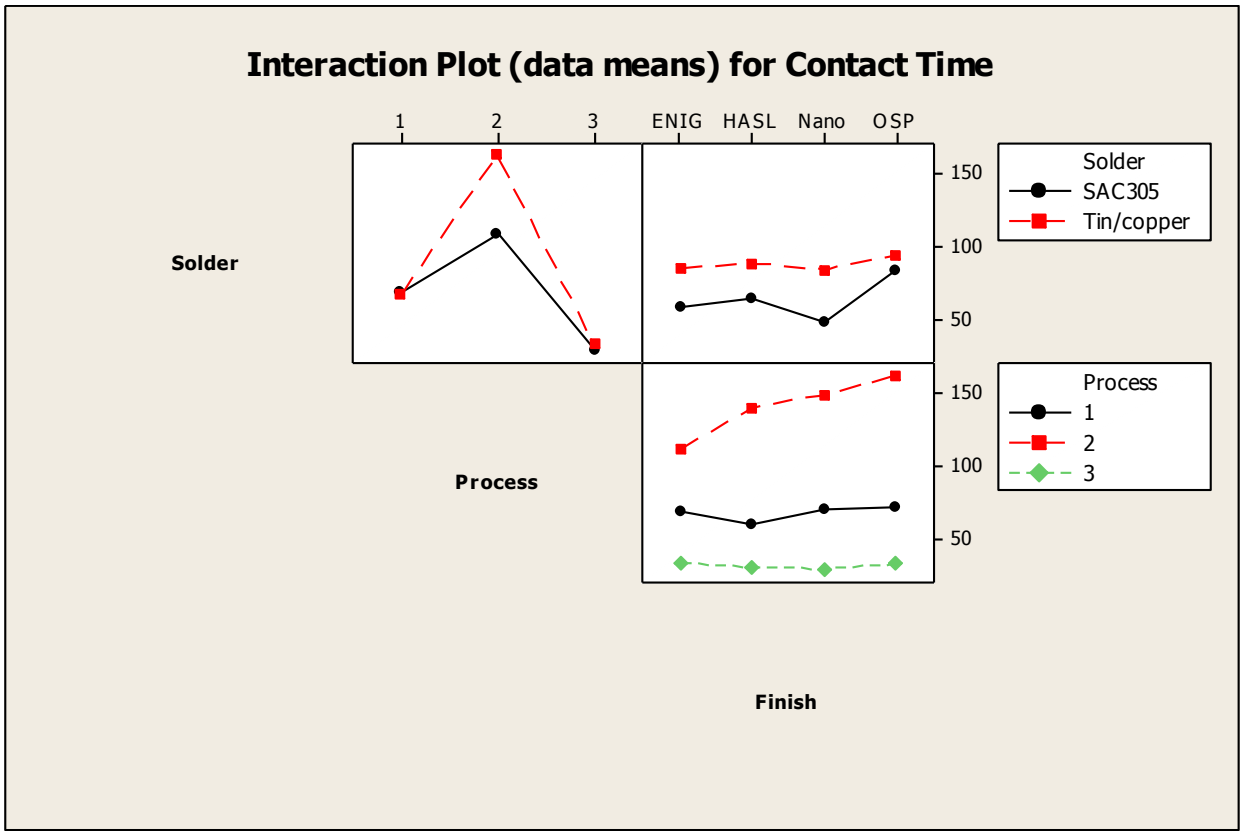

Figure 6.11. **Interaction plot for contact time.**

Copper Dissolution

The key measurement used to assess the degree of copper dissolution during the rework process was the thickness of the copper at the knee location of the plated through hole. This measurement was taken during the micro-sectioning process.

Micro-sectioning is a labor intensive process, and only the necessary rework coupons were micro-sectioned in order to reduce labor needs for this research. Since rework coupons with an ENIG surface finish have a nickel barrier, copper dissolution is typically not considered an issue for these coupons. Consequently, micro-sections were taken on only two out of the six ENIG rework coupons to validate that this assumption was accurate.

The micro-sectioning was done at the same location on the 200 pin through hole connector for each of the rework coupons. The plated through hole with the most copper dissolution was selected for cross section pictures and copper thickness measurements.

The copper thickness at the bottom side knee location was considered to be the minimum thickness of the copper for the rework coupon. The bottom side knee copper thickness was compared to IPC 6012B "Qualification and Performance Specification for Rigid Printed Boards" standards for minimum copper thickness [27]. The target level for the rework efforts was to achieve a Class 3 level which is a minimum

of 1.0 mil copper thickness. The IPC 6012B standards for minimum copper thickness are provided below. There were no signs of thermal degradation to the laminate or the component during the rework process.

- Class 3: minimum of 0.001" copper (1.0 mil)
- Class 2: minimum of 0.0008" copper (0.8 mils)
- Class 1: minimum of 0.0006" copper (0.6 mils)

The Main Effects Plot (Figure 6.12) was generated to show the copper dissolution measurements in relation to the solder alloy used, the rework process used, and the surface finish on the rework coupon.

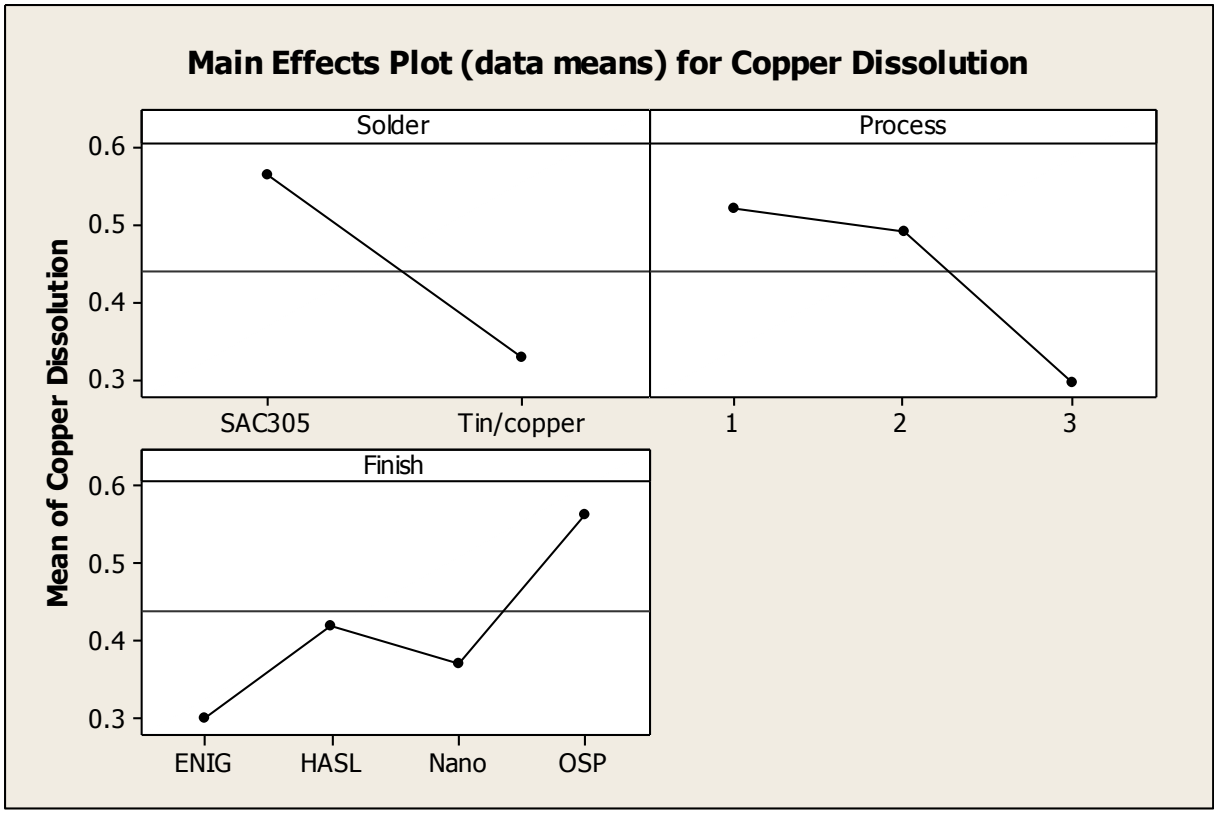

Figure 6.12. **Main effects plot for copper dissolution.**

Upon review of the Main Effects Plot for Copper dissolution, the following results were obtained.

- Tin/copper solder had 42% less copper dissolution than SAC305 solder.
- The hybrid nozzle used in Process 2 had 6% less copper dissolution than the standard nozzle used in Process 1.
- Use of the Air-Vac for component removal (Process 3) provided 43% less copper dissolution than Process 1.

- ENIG had the lowest copper dissolution, and the nano surface finish had the least amount of copper dissolution for a surface finish without a nickel barrier.

6.4.4 Reliability Testing Results

For the purposes of analyzing the results of the thermal cycling data, a minimum of 63% failures was required in order to plot the Weibull distribution. Therefore, the Weibull distribution was only provided for the component types that achieved a minimum of 63% failures during thermal cycling. Once the Weibull plot was generated for a component type, then various points of interest were calculated, such as the number of cycles to 1% cumulative failure (N_1), number of cycles to 50% cumulative failure (N_{50}), or characteristic life (N_{63}).

The thermal environment experienced by the test vehicle during thermal cycling was much different than the thermal environment of normal operating conditions. After the Weibull distribution was completed and the various points of interest were calculated in relation to number of thermal cycles, then the results were extrapolated to relevant use environments. There are numerous use environments depending upon the intended application of the electronic assembly.

Acceleration factors were required to convert life expectancies in the thermal chamber test environment to life expectancies for normal use environments or field conditions. There were several models developed for predicting the fatigue life of solder joints; the Norris-Landzberg model was selected for this research effort.

The Norris-Landzberg model is a sophisticated model that takes into account the effects of creep and stress relaxation. The model also takes into account the cyclic frequencies and the temperature-dependent properties of solder. The Norris-Landzberg model can be used for predicting the fatigue life of both tin/lead and lead-free solder joints. This model requires that the test vehicle and the product in field operations have the same material properties and design parameters. [28] The formula for the acceleration factor (AF) used in this model is as follows: [29], [22]

$$AF = N_O / N_t$$

$$AF = (\text{delta } T_t / \text{delta } T_O)^B * (t_t / t_O)^Y * \exp \{ (E_a/k * (1 / T_{max,O} - 1/T_{max,t})\} \quad (9)$$

where AF = Acceleration Factor

N_O = Number of cycles to failure (operation conditions)

N_t = Number of cycles to failure (test conditions)

T_t = Temperature (test conditions)

T_O = Temperature (operation conditions)

B, Y = fitting parameters

t_t = Time duration of thermal cycle (test conditions)

t_O = Time duration of thermal cycle (operation conditions)

E_a = Activation energy

k = Boltzman's constant

$T_{max,O}$ = Maximum temperature (operation conditions)

$T_{max,t}$ = Maximum temperature (test conditions)

The first term in the Norris-Landzberg equation accounts for the effect of temperature range for both the test and operation conditions. The second term in the Norris-Landzberg equation accounts for the effect of time duration. The third term in the Norris-Landzberg equation accounts for the effect of the maximum temperature.

The values for B, Y, and E_a/k in the Norris-Landzberg model were well studied and available in literature. However, the values for B, Y, and E_a/k were not as available for lead-free solders. In 2006, Pan et al. conducted research to develop values for B, Y, and E_a/k in the Norris-Landzberg model for SAC solder joints for three different surface mount component package styles: ceramic ball grid arrays (CGGA), chip scale package (CSP), and thin small outline package (TSOP). The B, Y, and E_a/k values used for tin/lead solders and the values developed by Pan et al. for SAC solder are provided in Table 6.2. [30] These values were used for determining the acceleration factor for both the tin/lead and SAC solder pastes used for this research.

Table 6.2: *Norris-Landzberg Exponents*

Parameter	Tin/Lead Solder	Lead-free (SAC) Solder
B	1.9	2.65
Y	0.33	0.136
E_a/k	1,414	2,185

The thermal cycling test included eighteen test vehicles: two test vehicles with halogen-free laminate material, and sixteen test vehicles with High Tg FR4 laminate material that were included in the Design of Experiments. The two test vehicles with halogen-free laminate material had early failures for all components. The components on the two test vehicles with halogen-free laminate material had all failed by 220 thermal cycles.

The thermal cycling data was recorded, collected, and analyzed for 1,470 thermal cycles. A summary of the thermal cycling failure data for the sixteen test vehicles in the Design of Experiments is provided in Table 6.3 for the daisy chains connected to only one component.

Table 6.3: *Thermal Cycling Data for Daisy Chains with One Component*

Component RefDes	Component Type	Number of Failures	Number of Daisy Chains	Percent Failed
U16	Chip array BGA, 100 balls (1.0 mm pitch)	12	16	75.0%
U17	Tape array microBGA, 64 balls (0.5 mm pitch)	9	16	56.3%
U26	Ceramic microBGA, 84 balls (0.5 mm pitch)	8	16	50.0%
U1, U2, U24, U25	TSOP, 48 Pins	13	56	23.2%
U15	PQFP, 208 pins	1	16	6.3%
U14, U18	Plastic BGA, 256 balls (1.0 mm pitch)	1	32	3.1%

The component located at reference designator U16 was the first component to surpass the 63% threshold. Twelve out of the sixteen test vehicles from the Design of Experiments had failures with the U16 component. This resulted in a 75.0% failure rate that exceeds the 63% threshold. Therefore, the Weibull distribution, acceleration factor, and operational life estimates were generated for this component.

The tape array microBGA (64 balls) component had the second highest failure rate at 56.3%. The plastic BGA with 256 balls appeared to be the most robust component type. It had the lowest failure rate of all components at 3.1%. Only one failure was detected for the 32 components included in the thermal cycling. One component lasted for 903 cycles before failure occurred.

The other components included in the thermal cycling were the surface mount resistors. Each of these components only had two solder joint terminations per component, whereas the components in the table above had between 48 to 256 solder joint connections per component. Therefore, the expected life for these components is very high and as a result there were multiple resistor components connected in series for each daisy chain circuit. It is only possible for the data logger to identify the first component failure for each daisy chain circuit. A summary of the thermal cycling failure data after 1,470 thermal cycles is provided in Table 6.4 for the daisy chains connected to more than one component.

Table 6.4: Therm*al Cycling Data for Daisy Chains with More Than One Component*

Component Type	Quantity of Components per Daisy Chain	Number of First Failures	Number of Daisy Chains	Percent of Daisy Chains with First Failure
0805 Resistor	49 - 52	23	32	71.9%
0402 Resistor	100	8	16	50.0%
0603 Resistor	100	7	16	43.8%

The three different resistors (0805, 0603, and 0402) were industry standard packages. These components had the same component finish and were made by the same manufacturer. The primary difference between the resistors is physical size. The 0805 resistor was the largest, and the 0402 resistor was the smallest. The 0402 resistor had the highest percentage (71.0%) of daisy chains where the first failure was identified. The U16 component is a surface mount component that is a chip array ball grid array.

The cycles to failure for the U16 component for each of the test vehicles included in the thermal cycling are shown in Table 6.5.

Table 6.5: *U16 Thermal Cycling Failure Data*

Test Vehicle	Solder Paste	PCB Laminate	Surface Finish	Failure Cycle
2	SAC 305 NC-1	High Tg FR4	ENIG	216
4	SAC 305 NC-1	High Tg FR4	LF HASL	522
6	SAC 305 NC-1	High Tg FR4	OSP	1 to 78
8	SAC 305 NC-1	High Tg FR4	Nanofinish	1 to 78
10	SAC 305 OA	High Tg FR4	ENIG	No failure found
12	SAC 305 OA	High Tg FR4	LF HASL	No failure found
14	SAC 305 OA	High Tg FR4	OSP	1 to 78
16	SAC 305 OA	High Tg FR4	Nanofinish	123
18	SAC 305 NC-2	High Tg FR4	ENIG	1 to 78
20	SAC 305 NC-2	High Tg FR4	LF HASL	899
22	SAC 305 NC-2	High Tg FR4	OSP	1 to 78
24	SAC 305 NC-2	High Tg FR4	Nanofinish	1 to 78
26	Tin/lead NC	High Tg FR4	ENIG	870
28	Tin/lead NC	High Tg FR4	LF HASL	196
30	Tin/lead NC	High Tg FR4	OSP	642
32	Tin/lead NC	High Tg FR4	Nanofinish	No failure found
34	SAC 305 NC-1	Halogen free	OSP	1 to 78
36	SAC 305 OA	Halogen free	OSP	1 to 78

Weibull probability plots were used to model the failure data obtained during the thermal cycling testing. The Weibull distribution was defined by two parameters, shape and scale. The shape parameter described the shape of the Weibull curve. A shape value of "3" approximated a normal curve. A shape value between "2" and "4" was still somewhat normal. A shape value lower than two low described a right-skewed curve, and a shape value greater than four described a left-skewed curve. The scale parameter is the 63.2 percentile ($N_{63.2}$) of the data. The scale parameter is sometimes referred to as

characteristic life. The scale value defines the position of the Weibull curve relative to the threshold. For example, a scale value of 10 indicates that 63.2% of the equipment will fail in the first 10 units (hours, cycles, etc.) following the threshold time.

The thermal cycling data for cycle numbers 2 through 78 was overwritten by the data logger. However, after cycle number 78, the exact failure cycle was recorded for each failed daisy chain circuit. Since there were failures that occurred somewhere between cycles 2 through 78 during the thermal cycling, the arbitrary censoring functionality was used in Minitab to generate the Weibull plot. For this functionality, Minitab used the least squares estimation method to calculate the Weibull distribution.

Eight out of the twelve lead-free test vehicles had experienced failures for the U16 component. The shape parameter calculated for U16 on lead-free test vehicles was 0.54, and the scale parameter calculated for U16 on lead-free test vehicles was 932.7.

All of the four tin/lead test vehicles had experienced failures for the U16 component. The shape parameter calculated for U16 on tin/lead test vehicles is 1.06, and the scale parameter calculated for U16 on tin/lead test vehicles is 718.3.

The Weibull distribution was used to determine the percent of test vehicles that were anticipated to fail by a particular time under test conditions. In this case, it was the percent of test vehicles that were anticipated to fail by a certain number of thermal cycles under test conditions. The Table of Percentiles provided by Minitab for both the lead-free and tin/lead test vehicles for the U16 component is provided in Table 6.6.

Table 6.6: *Table of Percentiles for U16 Component*

Percent	Designation	Lead-free Percentile	Tin/lead Percentile
1	N_1	0.2	9.4
10	N_{10}	15.0	85.9
20	N_{20}	59.3	174.4
30	N_{30}	140.4	271.5
40	N_{40}	271.6	381.1
50	N_{50}	475.8	508.3
60	N_{60}	794.3	661.5
63.2	$N_{63.2}$ (scale value)	932.7	718.3
70	N_{70}	1,311.6	855.9
80	N_{80}	2,235.2	1,125.6
90	N_{90}	4,314.9	1,578.1

This information can be interpreted, for example, that 10% (N_{10}) of the U16 components on tin/lead test vehicles will fail during thermal cycling conditions after approximately 86 thermal cycles, and 70% (N_{70}) of the U16 components on lead-free test vehicles will fail during thermal cycling conditions after approximately 1,311 thermal cycles. For the component U16, the tin/lead test vehicles appeared more

robust from N_1 through N_{50}. However, there was a crossover point after N_{50}, and from N_{60} through N_{90} the lead-free test vehicles appear more robust. This indicated that there may be two different failure modes involved, one possibly an infant mortality related failure mode and the other possibly a wear out mechanism failure mode. [31] This is further evidence for this situation in that there were four lead-free test vehicles that have not had failures for the U16 component, but there have been U16 failures to date for all four of the tin/lead test vehicles.

After the failure data for component U16 had been characterized for thermal cycling conditions, it was necessary to extrapolate the reliability performance from test conditions to actual operation conditions. Three actual operation conditions with reliability implications were chosen that were relevant to members of the Consortium: data center, automotive, and aerospace operation conditions. The minimum and maximum temperatures, as well as the cycle time frequency for these operation conditions, are provided in Table 6.7.

Table 6.7: ***Test and Operation Conditions***

Application	Minimum Temp.	Maximum Temp.	Temp. Cycles per Day	Temp Cycle Duration
Thermal Cycling (Test)	- 55 ^{o}C	+ 125 ^{o}C	14.1	102 minutes
Aerospace	- 40 ^{o}C	+ 125 ^{o}C	14 - 16	90 – 102.8 minutes
Automotive	- 40 ^{o}C	+ 85 ^{o}C	2 - 5	288 – 720 minutes
Small Business IT Systems	+ 10 ^{o}C	+ 70 ^{o}C	2	720 minutes

The Norris-Landzberg model was used to calculate the acceleration factor for each of the three operation conditions above. The higher end of the range of the temperature cycles per day were used for the aerospace and automotive applications. The acceleration factors calculated were as follows:

Aerospace: 1.1

Automotive: 4.2

Data Center: 27.2

The acceleration factor calculated for the aerospace application (1.1) was close to one because the aerospace conditions were very similar to the test conditions for minimum temperature, maximum temperature, and temperature cycles per day. The acceleration factor calculated for the data center application (27.2) was much greater than one because the data center operation conditions were very different than the test conditions for minimum temperature, maximum temperature, and temperature cycles per day.

The next step taken was to apply the acceleration factor to the N_x expected life during test conditions to calculate the N_x for actual product life for various applications. The anticipated product life for lead-free test vehicles in aerospace, automotive, and small business IT systems applications is provided in Table 6.8.

Table 6.8: *Product Life For Lead-free Solders*

Application	Acceleration Factor	N_{10} Test Cycles	N_{10} Operation Cycles	$N_{63.2}$ Test Cycles	N_{50} Operation Cycles
Aerospace	1.2	15	18	933	1,120
Automotive	5.6	15	84	933	5,225
Small Business IT Systems	57.8	15	867	933	53,927

The anticipated product life for tin/lead test vehicles in aerospace, automotive, and small business IT systems applications is provided in Table 6.9.

Table 6.9: *Product Life For Tin/Lead Solders*

Application	Acceleration Factor	N_{10} Test Cycles	N_{10} Operation Cycles	$N_{63.2}$ Test Cycles	N_{50} Operation Cycles
Aerospace	1.1	86	95	718	790
Automotive	4.2	86	361	718	3,016
Small Business IT Systems	27.2	86	2,339	718	19,530

For the U16 component, it can be seen that the operation cycles were much higher for all applications for the test vehicles that were made with the tin/lead solder as compared to the test vehicles made with lead-free solder. For example, the N_{10} operation cycles for the automobile application using lead-free solder was 86 cycles, while the operation cycles for tin/lead solder was 361 cycles.

Nineteen out of the twenty-four lead-free daisy chains with the 0805 component have experienced failures. The shape parameter calculated for U16 on lead-free test vehicles was 5.3, and the scale parameter calculated for U16 on lead-free test vehicles was 886.8.

Four out of the eight tin/lead daisy chains with the 0805 components have experienced failures. The shape parameter calculated for U16 on tin/lead test vehicles was 2.4, and the scale parameter calculated for U16 on tin/lead test vehicles was 1,660.7.

The Weibull distribution was used to determine the percent of test vehicles that were anticipated to fail by a particular time under test conditions. The Table of Percentiles provided by Minitab for both the lead-free and tin/lead test vehicles for the 0805 component is provided in Table 6.10.

Table 6.10: ***Table of Percentiles for 0805 Component***

Percent	Designation	Lead-free Percentile	Tin/Lead Percentile
1	N_1	370.8	244.3
10	N_{10}	578.8	650.3
20	N_{20}	667.3	889.0
30	N_{30}	729.4	1,080.8
40	N_{40}	780.8	1,255.3
50	N_{50}	827.3	1,425.5
60	N_{60}	872.2	1,601.3
63.2	$N_{63.2}$ (scale value)	886.8	1,660.7
70	N_{70}	918.6	1,794.3
80	N_{80}	970.5	2,024.9
90	N_{90}	1,038.7	2,350.8

For the 0805 component, the lead-free test vehicles appeared more robust than the tin/lead test vehicles for the N_1 percentile. However, there was a crossover point after N_1, and from N_{10} through N_{90} the tin/lead test vehicles appeared more robust. This indicated that there may be two different failure modes involved, one possibly an infant mortality related failure mode and the other possibly a wear out mechanism failure mode.

6.5 Conclusions

This section outlines the conclusions for the assembly of test vehicles, rework with lead-free materials, and the reliability of lead-free electronics.

6.5.1 Assembly

Surface Mount Component Assembly

The test vehicles assembled with the SAC 305 NC1 solder paste had the lowest defect rate for all the solder pastes evaluated in this research. For test vehicles assembled with lead-free solder pastes, the nano and lead-free HASL surface finishes had the lowest defect rates. For the various lead-free solder paste and surface finish combinations, the combination of SAC305 NC1 solder paste and the HASL surface finish had the overall lowest defect rate for the test vehicles assembled for this research.

Through-Hole Component Assembly

Overall, the test vehicles assembled with the tin/copper (1) solder had the lowest defect rate for all three through-hole component solders evaluated in this research. For boards assembled with lead-free solders, tin/copper (1) solder had the lowest defect rate, and the HASL surface finish had the lowest defect rate. There was significant variation in the performance of the ENIG surface finish with the

various solders. For the tin/lead and SAC305 solders, ENIG was the surface finish with the least defects, and for both tin/copper solder parameters, ENIG was the surface finish with the most defects. The lead-free HASL surface finish provided the most consistent results as it had either the lowest or second lowest defect rate across all solders.

For through-hole component assembly, the test vehicles assembled with the OSP and nano surface finishes had the highest level of defects. For the test vehicles with an OSP finish, a contributor to this high failure rate was the time delay between conducting the surface mount assembly and through-hole assembly. During this delay, the OSP surface finish could potentially degrade, which could have a negative impact on subsequent soldering efforts. A key recommendation was to try to minimize the time delay between surface mount and through-hole component assembly efforts. Preferably, both procedures should be conducted during the same day.

The best method for applying the nano surface finish to printed circuit boards was to apply it directly to bare copper. However, for the test vehicles used in this research, this method was not followed. Instead, an OSP finish had been previously applied to the test vehicle, then the OSP finish was stripped off, and then the nano surface finish was applied to the test vehicles. The soldering results would most likely be better if the nano surface finish was applied directly to bare copper for further research or assembly efforts.

6.5.2 Rework

Contact Time

Contact time between the test vehicle and the liquid solder in the rework nozzle can be a contributing factor to the generation of copper dissolution. In general, a greater contact time results in greater copper dissolution, if all other contributing factors (e.g., solder, surface finish, nozzle design, etc.) are equal. Process #1 had a much lower mean contact time as compared to the mean contact time for Process #2. The only difference between these two processes was the type of nozzle used, where Process #1 used the standard nozzle and Process #2 used the hybrid nozzle. Therefore, the contact time required for solder flow through to the topside of the rework coupon was much greater for the hybrid nozzle than for the standard nozzle.

Process #3 had the lowest mean contact time, which can be attributed to no contact time during the component removal process when using the Air-Vac machine. The SAC 305 solder had a much lower mean contact time as compared to tin/copper. The contact time for the ENIG was the lowest of the four surface finishes, and the nano surface finish was the lowest of the three other surface finishes without a nickel barrier. The combination of process and surface finish with the lowest contact time was Process #3 with the nano surface finish.

Copper Dissolution

The target objective for the rework efforts was to achieve IPC 6012B Class 3 standards for a minimum copper thickness of 1.0 mils or greater. This target was achieved for several rework coupons that underwent rework with lead-free solder and surface finishes. The rework coupons that used the

tin/copper solder had greater contact time but less copper dissolution than the coupons using the SAC305 solder for the rework efforts. Therefore, the type of solder alloy was a greater contributing factor to copper dissolution than the contact time.

The rework coupons that used Process 2 (hybrid nozzle) had greater contact time but less copper dissolution than Process 1 (standard nozzle). Therefore, the hybrid nozzle was effective at reducing the copper dissolution even though it required additional contact time. The rework coupons that used Process 3 had less contact time and less copper dissolution than both Process 1 and Process 2. The reduction in contact time is attributed to the use of the Air-Vac equipment for the component removal. The rework coupons with the ENIG surface finish had the lowest copper dissolution because of the protective nickel barrier. The rework coupons with the nano surface finish had the least amount of copper dissolution for a surface finish without a nickel barrier. Finally, there were no signs of thermal degradation to the laminate or the components during the rework efforts.

6.5.3 Reliability

The test conditions within the thermal cycling chamber were much more severe than most operating environments for electronic products. The intent was to accelerate aging and produce early failures. The two test vehicles with halogen-free laminate material had early failures for all components. The components on the two test vehicles with halogen-free laminate material had all failed by 220 thermal cycles. Therefore, there appeared to be major reliability issues with the halogen-free laminate based upon the thermal cycling test conditions used in this research.

The sixteen test vehicles included in the Design of Experiments used the high Tg FR4 laminate material and had proven to be robust. Only two out of the nine different component types being monitored for failures had exceeded the 63% failure threshold after experiencing 1,470 thermal cycles. The U16 BGA component was the first component to achieve greater than the 63% failure threshold for the sixteen test vehicles included in the Design of Experiments. Based upon the Weibull plot results for the U16 component, the tin/lead test vehicles appeared more robust from the percentiles N_1 through N_{50}. However, there was a crossover point after N_{50}, and from N_{60} through N_{90} where the lead-free test vehicles appeared more robust. This indicated that there may be two different failure modes involved, one possibly an infant mortality related failure mode and the other possibly a wear out mechanism failure mode.

The 0805 resistor was the second component to achieve greater than the 63% failure threshold for the sixteen test vehicles included in the Design of Experiments. For the 0805 component, the lead-free test vehicles appear more robust than the tin/lead test vehicles for the N_1 percentile. However, there was a crossover point after N_1, and from N_{10} through N_{90} the tin/lead test vehicles appeared more robust.

7.0 SUMMARY

Based on the assembly results achieved by the New England Lead-free Electronics Consortium, with the careful selection of solder paste and surface finish, it was demonstrated that surface mount and through-hole components can be assembled with lead-free materials and achieve a rate of defect equal to or less than boards assembled with tin/lead materials. From a rework standpoint, the research was successful in demonstrating that rework with lead-free materials can meet IPC Class 3 standards for minimum copper thickness.

The cooperation and assistance provided by the members of the Consortium over the course of all four phases of this research was essential for its success. From an assembly perspective, the research conducted by the Consortium was successful in providing needed information to help companies transition to lead-free electronics assembly.

The success of the Consortium in this research project further demonstrated that toxics use reduction for complex products and assemblies can be accomplished by working with a supply chain. Also, this collaboration benefited the Consortium's academic, government, and industry participants. For example, the industry participants were able to have direct input and influence on the type of research that was undertaken, were able to share the costs to address a major industry challenge, and gained a competitive advantage in preparing to transition to lead-free electronics. The academic participants were able to forge collaborative relationships between the university and regional businesses and provide real-world learning opportunities for the graduate and undergraduate students that participated at various stages of the research. The government participants were able to reduce the use of a toxic material (lead) which helps create a safer occupational setting and an improved environment. Overall, the government, industry, and academia collaboration was a successful model for applying toxics use reduction principles to a challenging and important application. [32], [33]

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